# 1 MHz PWM GENERATION USING INTERSECTIVE METHOD

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By

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Dissertation submitted in partial fulfillment
of the requirements for the
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# CERTIFICATION OF APPROVAL

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(ELECTRICAL AND ELECTRONICS ENGINEERING)

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## CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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(MUHAMMAD AFIQ BIN MOHD SADLI)

# ABSTRACT

This project serves as a basis to investigate the performance of a PWM generator circuit. This is due to available PWM generation method cannot cover a wide operation frequency and wide duty cycle range. PWM signal had been used in various application including power system, communication and control systems. Pulse-width modulation (PWM) is a very efficient way of providing intermediate amounts of electrical power between fully on and fully off. A simple power switch with a typical power source provides full power only, when switched on. PWM is a comparatively-recent technique, made practical by modern electronic power switches. This project will focus on PWM generation in high frequency of 1 MHz. The aim of this work is to generate PWM signal at 1 MHz frequency with duty cycle ranging from 30 % to 70 %. During the process, various parameters like duty cycle, rise and fall time, and signal resolution is observed to determine the quality of PWM signal generated. From the findings, this work will determine the suitable conditions that can be implemented in suitable application using this PWM generation technique, intersective method.

# ACKNOWLEDGEMENT

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# LIST OF ABBREVIATIONS

Wherever applicable the meaning of each abbreviation used in this preliminary report is given. The abbreviations in the following list are most widely used throughout this preliminary report.

**Abbreviations**

| | | |
|---|---|---|
| AC | - | Alternating current |
| DC | - | Direct current |
| IC | - | Integrated circuit |
| OP-AMP | - | operational amplifier |
| NPN | - | Negative-Positive-Negative |
| MOSFET | - | metal–oxide–semiconductor field-effect transistor |

# CHAPTER 1

# INTRODUCTION

## 1.1 Background of Study

Pulse Width Modulation (PWM) is the widely used technique various switching applications. The implementation of PWM over traditional linear switching is preferable as the switching loss ($I^2R$ loss) found in traditional linear switching is not present in PWM switching. Pulse-width modulation (PWM) is a very efficient way in providing intermediate amounts of electrical power between fully on and fully off. A simple power switch with a typical power source provides full power only, when switched on. PWM is a comparatively-recent technique, made practical by modern electronic power switches, in example; switching of MOSFETs in power electronic converters namely AC to DC converter (rectifier), DC to AC converter (inverter), DC to DC converter (chopper) and AC to AC converter (cycloconverter).

Pulse-width modulation (PWM) of a signal or power source involves the modulation of its duty cycle, to either convey information over a communications channel or control the amount of power sent to a load.

In this work, PWM is generated using intersective method by comparing the sawtooth waveform as modulating signal and DC level voltage as reference voltage in 1 MHz frequency.

## 1.2 Problem Statements

The available means of PWM generation is basically restricted in terms of operating frequency (usually low frequency) and duty cycle ranges. Apart from that, the complexity of the circuit and the cost itself is the main drawback of generating high frequency PWM signal. The first challenge of this project is how to generate PWM signal at 1 MHz frequency with varying duty cycles ranging from 30 % to 70 %. PWM signal is derived from sawtooth waveform. So, it is important to study how sawtooth waveform is generated and then manipulating the signal using several methods to get PWM signals. The sawtooth waveform is derived from the function generator and PWM generator circuit is built to get 1 MHz PWM signal. This work will investigate the performance of the proposed circuit in terms of range of duty cycles and the resolutions of PWM signals in 1 MHz frequency. This work will be verified with several PWM chips found in the market.

## 1.3 Objective and Scope of Study

The objective of this study is to determine whether the proposed PWM generator circuit is able to perform in 1 MHz with wide range of duty cycle and have good resolution. Sawtooth waveform as the modulating signal in PWM circuit will be studied as well. This includes the study of various ways to generate sawtooth signal and make comparison between the methods. The scope of study will cover the theory of PWM generation and the theory of operation of the proposed circuit. The quality of generated PWM signal will be observed in terms of resolution and noise.

# CHAPTER 2

# LITERATURE REVIEW

## 2.1 PWM Signal

PWM is important to control power switches as it provides intermediate electrical power between fully on and fully off. The interval during fully on time will determine the amount of power being transferred by the power switch. The proportion of on time in regular interval or period of time is termed as duty cycle and express in percentage. 100% means the switch is being fully switched on while 0% means the switch is being fully switch off. Hence, the duty cycle value determines the amount of power transferred [1]. Duty cycle is directly proportional to the amount of power transferred. So, low duty cycle indicates low power and high duty cycle indicates high power. Duty cycle, $D$ is given by:

$$D = \frac{\tau}{T} \tag{1}$$

Where $\tau$ = duration of time when fully ON

$T$ = the period of the function

The PWM in this project is obviously applied for power application in the converter circuit. PWM has several advantages [2] of normal switching method. PWM provides lesser power loss during switching (power loss in the form of heat from $I^2R$ losses), faster switching hence high frequency circuit application is possible and relatively low cost as the devices needed is lesser and the circuit construction is made simpler with the use of semiconductor switches and devices.

## 2.2 Sawtooth Waveform

Sawtooth waveform is used as modulating signal in PWM generation. Sawtooth waveform is a kind of non-sinusoidal waveform. The name sawtooth is derived from its resemblance to the teeth on the blade of a saw. Sawtooth wave ramps upward and then sharply drops.

The general mathematical form of sawtooth waveform, is based on the floor function of time $t$, in the range $-1$ to 1, and with period $a$, can be expressed in (2) below:

$$x(t) = 2\left(\frac{t}{a} - \text{floor}\left(\frac{t}{a} - \frac{1}{2}\right)\right) \tag{2}$$

RMS voltage, $V_{rms}$ and average voltage, $V_{avg}$ in sawtooth signal is related with peak voltage, $V_{pk}$, frequency, $f$ and duration of the signal itself [3]. The RMS voltage, $V_{rms}$ is expressed in (3) below:

$$V_{rms} = V_{pk}\sqrt{\frac{fT}{3}} \tag{3}$$

As for average voltage, $V_{avg}$, it is expressed in (4) below:

$$V_{avg} = \frac{V_{pk} \times T \times f}{2} \tag{4}$$

Sawtooth signal is derived directly from the function generator which is set at 1 MHz frequency and fed to the inverting input of the OP-AMP or comparator in the PWM generator circuit.

## 2.3 Comparator

A comparator is an electronic device which compares two voltages or currents and switches its output to indicate which is larger. The operational amplifier or op-amp is suitable way to implement voltage comparator as it has a well balanced difference input and high gain [4]. These characteristics allow the op-amps to serve as comparator. To make op-amp to operate as comparator, the op-amp should operate in open-loop configuration.

The output of op-amp will be at the most positive voltage when non-inverting input voltage (V+) is higher than inverting input (V-). Otherwise, the op-amp output is at the most negative voltage it can when the non-inverting input (V+) drops below the inverting input (V-).

## 2.4 Comparator Feedbacks

The effect of output in different feedback configuration in the op-amp also needs to be investigated to determine the suitable feedback configuration that fits the purpose of this project.

### 2.4.1 Positive feedback

In this configuration, the output voltage is routed back to the non-inverting input as shown in Figure 1.

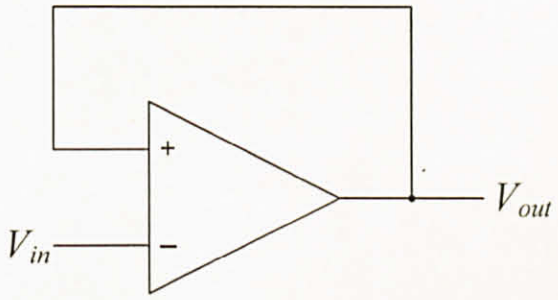



Figure 1 : Positive feedback comparator

In this configuration, the output tends to be in the state that its already in. A slight change in the voltage would not change the output state. The output state only occurs when the voltage is at the most positive or at the most negative input [5]. Therefore, we can say that it *latches* between one of the two states, saturated positive or saturated negative. This condition is known technically as *hysteresis*.

### 2.4.2 Negative feedback

This configuration is realized by connecting the output with the inverting input as shown in this Figure 4:

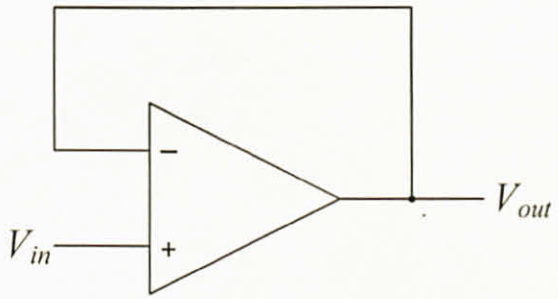



Figure 2: Negative feedback comparator

In this configuration, a voltage follower is created when op-amp is directly connected to the inverting input (-). Any signal voltage that is impressed to the non-inverting input will be seen at the output. With this feedback configuration, the op-amp will always try to drive the output voltage to any differential voltage necessary to make the voltage difference practically zero. It can be concluded that op-amp in this configuration always try to reach a point of equilibrium [6].

## 2.5 Transistor biasing

Transistors must be properly biased to ensure correct operation. Biasing is commonly consists of resistor networks. There are various ways of biasing transistor including fixed bias, self-bias and combination bias. In the proposed circuit, fixed bias technique is used. Using this bias method, a biasing resistor is connected between the collector supply, $R_C$ and the base, $R_B$ [7]. This is a very simple arrangement and the connection is shown in the Figure 3 below.

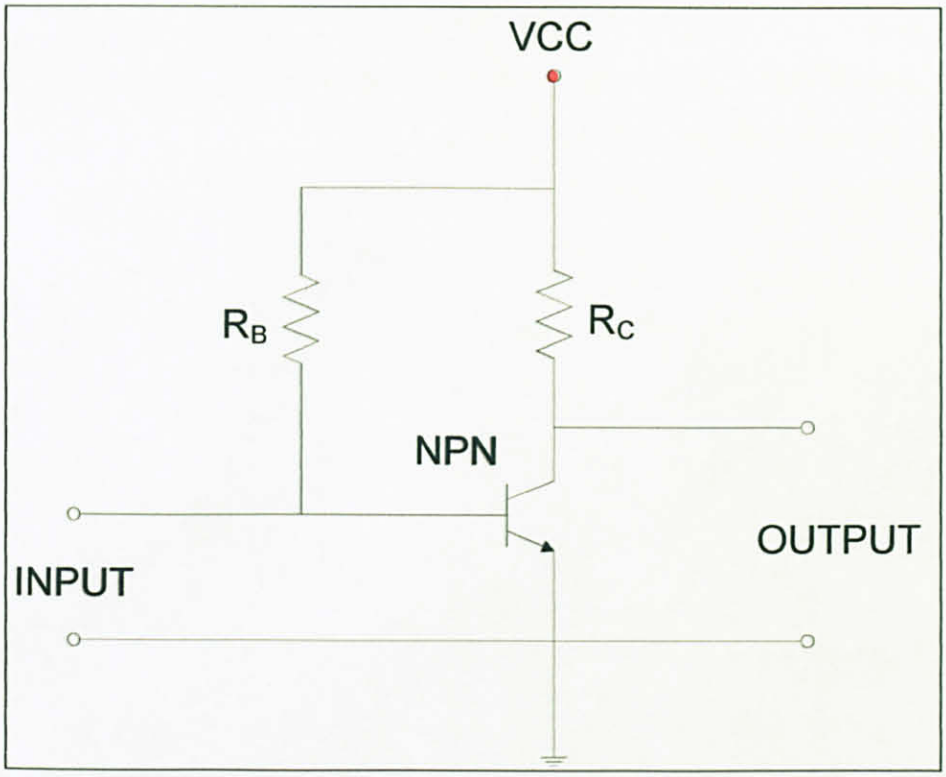



Figure 3 : Fixed biasing diagram

## 2.6 Common emitter connection

There are three ways that a transistor can be connected in a circuit: Common emitter, common base and common collector [7]. In this proposed circuit, the transistor is connected using common emitter connection. This transistor connection provides amplification of signal in the circuit. It features good voltage, current and power gain sufficient enough for this circuit's purpose. It has low input resistance. The input signal is applied between the base and the emitter, a low resistance and low current circuit. When the input signal goes to positive values, the base goes to positive values, decreasing the forward bias hence reducing the corrector current and increases the collector voltage. The collector current that flows through the high resistance reversed bias junction also flows through a high resistance load resulting in high level of amplification. The output signal goes negative when the input signal goes positive. The connection is shown in Figure 4 below.

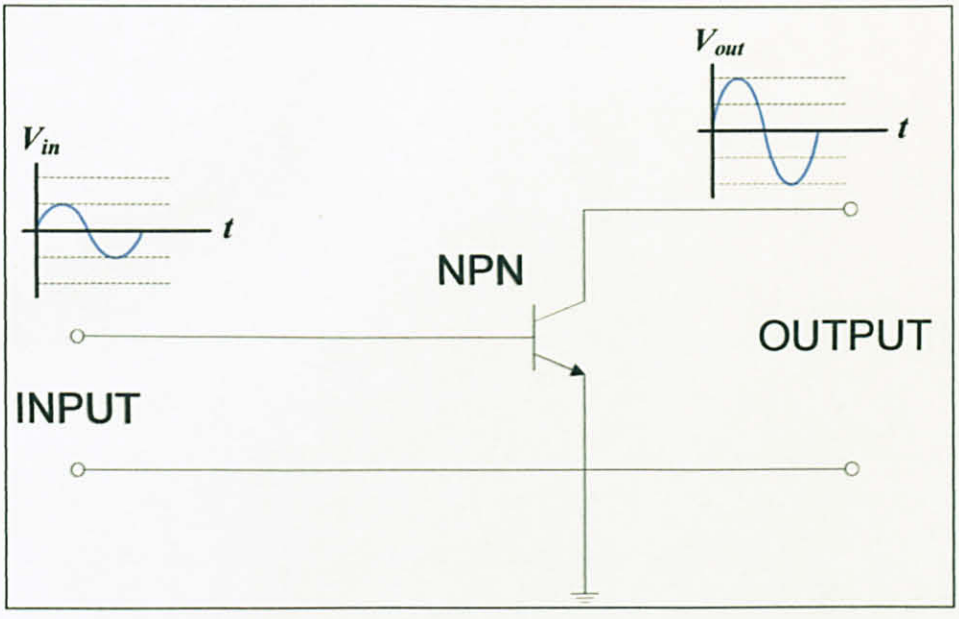



Figure 4 : Amplification using common emitter connection

The amplification amount is called Gain. It is the ratio of the output over the input. Different value of gain is obtained with different transistor configurations although the same transistor is used. The selection of configuration to be selected is subject to the type of application. The current gain, $\beta$ or also expressed as $h_{FE}$ in the common emitter connection is the relationship of collector current to base current as expressed in (5) below [8]:

$$h_{FE} = \beta = \frac{\Delta I_C}{\Delta I_B} \tag{5}$$

Resistance gain, $R$ is the ratio of output resistance and input resistance as expressed in (6) below:

$$R = \frac{R_{out}}{R_{in}} \tag{6}$$

Voltage gain, $E$ is the sum of current gain, $\beta$ multiplied by resistance gain, $R$ as expressed in (7) below:

$$E = \beta \times R \tag{7}$$

Power gain, $P$ is the sum of current gain, $\beta$ multiplied by voltage gain, $E$ as described in (8) below:

$$P = \beta \times E \tag{8}$$

## 2.7 Creation of PWM signal

To create PWM signal, the sawtooth waveform as modulation signal and DC sine waveform as reference signal are fed to the comparator as shown in Figure 5.

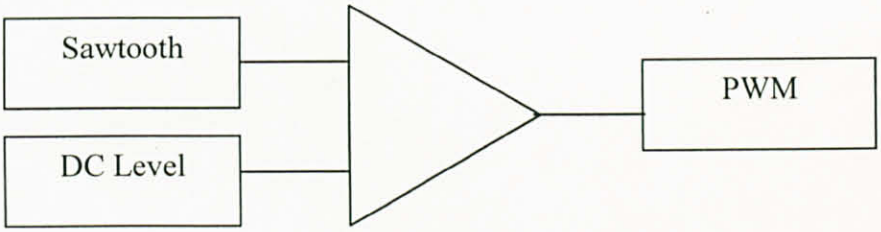



Figure 5 : PWM generator block diagram

This method is called intersective method [9]. When the value of DC reference signal (**green**) is greater than the sawtooth modulation signal (**red**) the PWM signal (**blue**) is in high state as shown in Figure 6. When the DC reference signal value is smaller than the sawtooth modulation signal, the PWM signal enters the low state. It is noted that the duty cycle width is determined by the reference voltage $V_{ref}$ of the DC level signal.

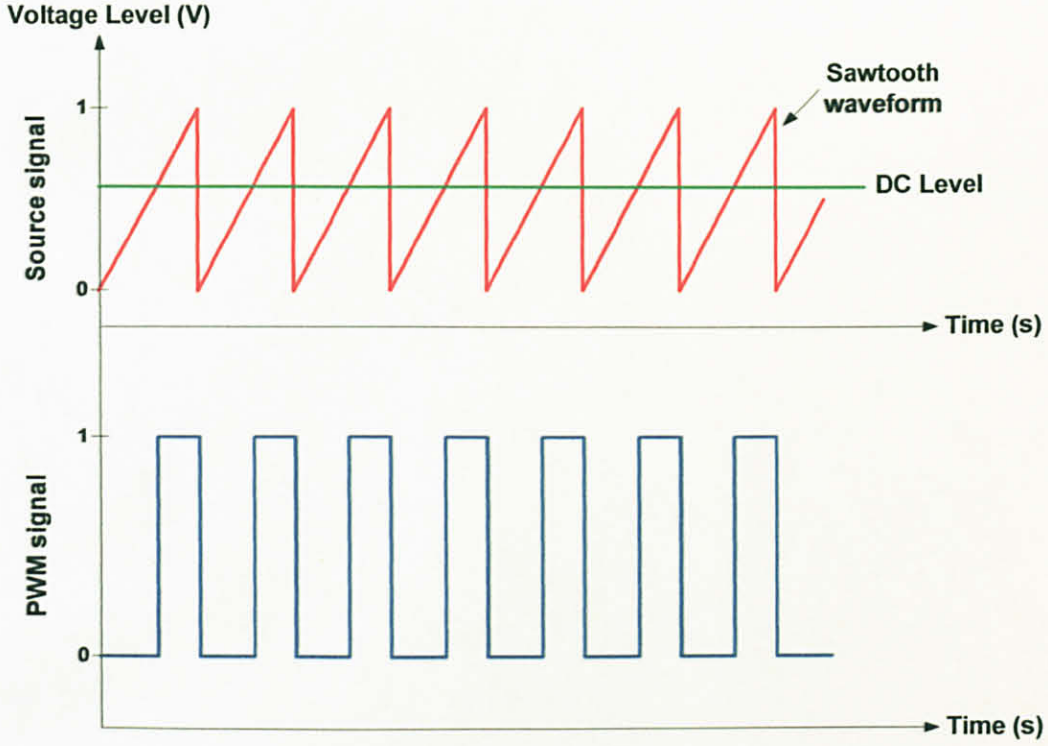



Figure 6: Source signal and PWM signal graph

## 2.8 Rise time and fall time

In practical application, the PWM signal is not perfectly a square wave. It will take some time to change from one voltage level to another known rise time, $t_r$ and fall time, $t_f$. Rise time, $t_r$ is the difference between the time when the signal crosses a low state to the time when the signal crosses the high state while fall time, $t_f$ is the difference between the time when the signal crosses a high state to the time when the signal crosses the low state [10]. This can be represented in Figure 7 below.

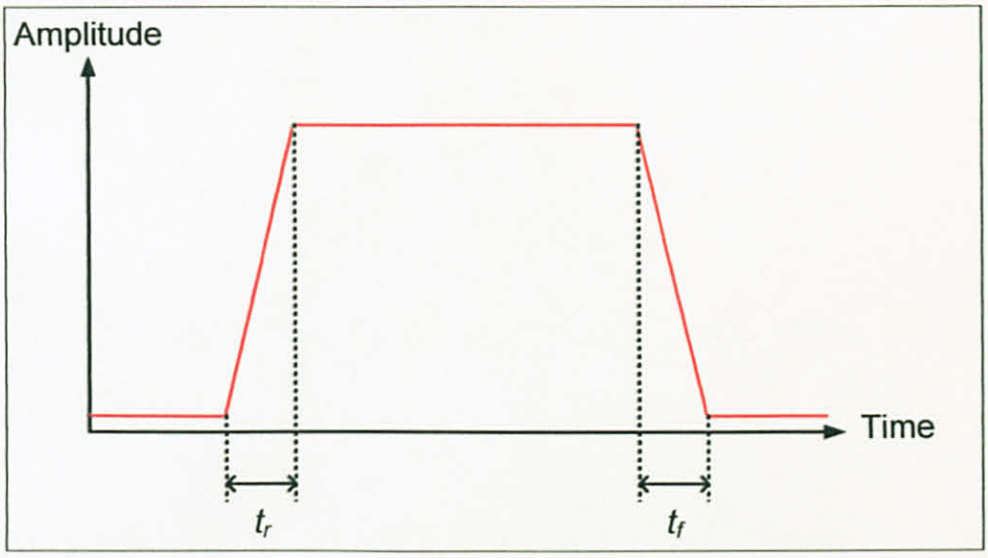



Figure 7 : Rise time and fall time in PWM signal.

## 2.9 Resolution of PWM signal

From rise time and fall time, the resolution of PWM signal can also be determined. The resolution of the signal determines the quality of the signal [11]. Resolution is the time taken between the 10% and 90% point of the rise time as shown in Figure 8 below.

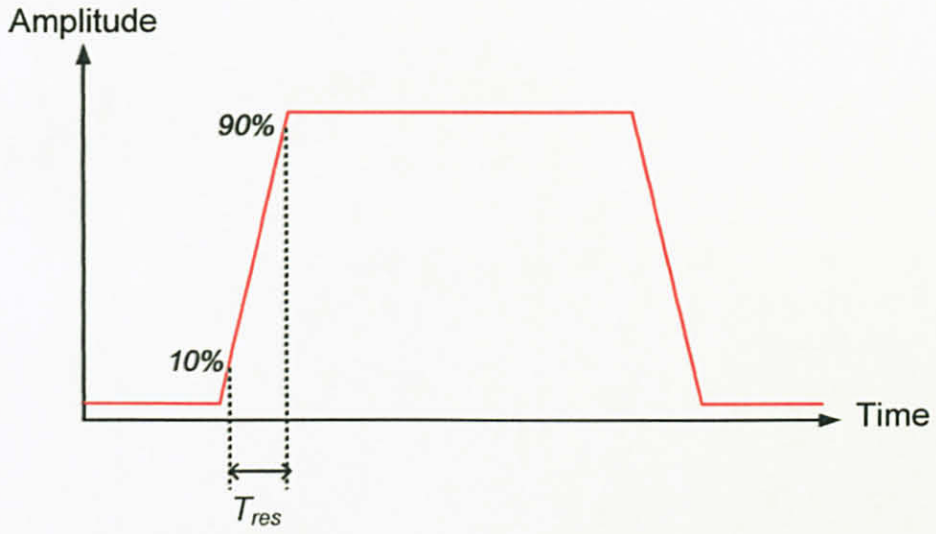


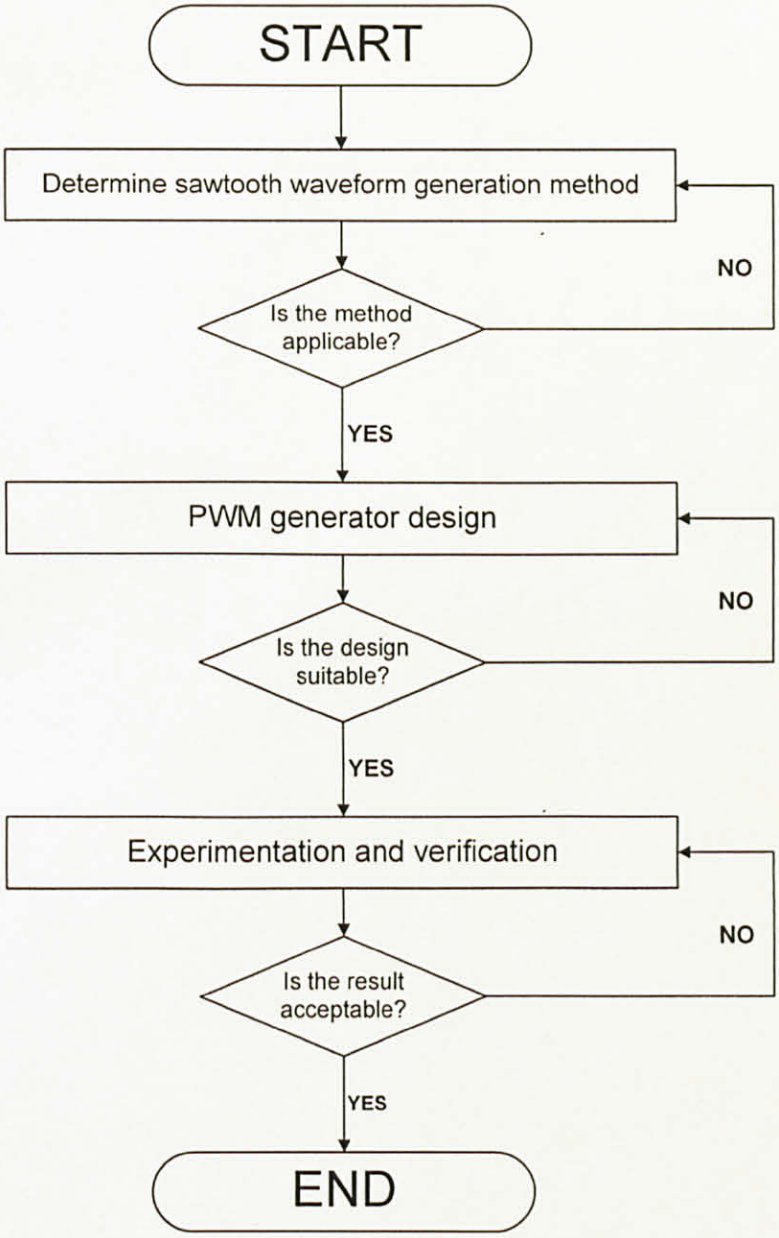

Figure 8 : Determining resolution of a PWM signal

Resolution is expressed in nanoseconds (ns). Smaller time (in nanoseconds) will give better resolution to the signal. In high frequency PWM, the resolution will be measured to determine the performance of PWM signal generation using intersective method at 1 MHz frequency.

# CHAPTER 3

# METHODOLOGY

## 3.1 Process Flowchart



### 3.2 Required Hardware

In this experimentation, the hardware is needed to build the related circuits for analysis and testing purposes.

Table 1 : Required hardware and software

| Hardware | Functions / Use |
|---|---|
| Voltage comparator (operational amplifier) | Compares sawtooth waveform input with DC level reference voltage to generate PWM signal. |
| Function generator | Produces needed waveform and signal for experimentation activities. |
| Oscilloscope | Captures the waveform in the circuit for analysis. |
| Digital Multimeter (DMM) | To take important readings (voltage, current, resistance etc.) on the physical circuit. |
| Printed Circuit Board (PCB) | Provide mean of building a circuit and customize it when needed. |

## 3.3 Components and Tools

### 3.3.1. Comparator

As for comparator, MAX944 is the component of choice [12]. The advantage of this comparator is it uses single supply thus reducing the circuit complexity. This IC houses for comparators that is suitable for generating multiple PWM signal. The basic specifications are as follows:

Supply voltage : 2.7V – 6.0V

Input voltage range : -0.2V to +0.2V

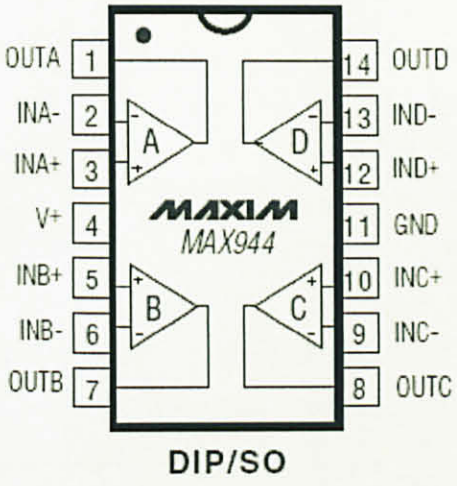



Figure 9: MAX944 pin layout [12]

### 3.3.2. Transistor Characteristics

For amplification purposes, the circuit uses PN2222A, NPN general purpose amplifier. This component can be used as a medium power amplifier for the circuit [13]. The important electrical characteristics are as follows:

Table 2 : On characteristics of PN2222A NPN transistor

| Symbol | Parameter | Test condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $h_{FE}$ | DC Current Gain | IC = 0.1mA, VCE = 10V | 35 | | |
| | | IC = 1.0mA, VCE = 10V | 50 | | |
| | | IC = 10mA, VCE = 10V | 75 | | |
| | | IC = 10mA, VCE = 10V, (Ta = -55°C) | 35 | | |
| | | IC = 150mA, VCE = 10V * | 100 | 300 | |
| | | IC = 150mA, VCE = 10V * | 50 | | |
| | | IC = 500mA, VCE = 10V * | 40 | | |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage | IC = 150mA, VCE = 10V | | 0.3 | V |
| | | IC = 500mA, VCE = 10V | | 1.0 | V |
| $V_{BE(sat)}$ | Base-Emitter Saturation Voltage | IC = 150mA, VCE = 10V | 0.6 | 1.2 | V |
| | | IC = 500mA, VCE = 10V | | 2.0 | V |

### 3.3.3. Sawtooth Generation

For the first attempt to generate sawtooth waveform, a circuit has been built as shown in Figure 10 below [14]:

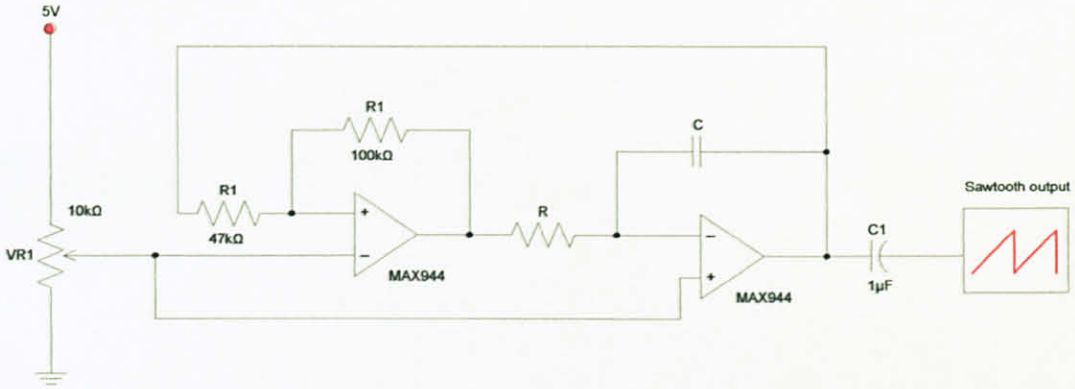



Figure 10 : Sawtooth generator circuit

The oscillation frequency of the triangle wave by choosing the suitable $R$ and $C$ values and they are related by equation 9:

$$f_{osc} = \frac{1}{2 \times R \times C} \tag{9}$$

However, it is difficult to precisely tune the circuit at 1 MHz. This is due to there are no component with correct value available and tolerance in resistor. The resistors actual values are measured using digital multimeter first to investigate the effect of component values to the frequency. The $R$ and $C$ value combinations are shown in Table 3.

Table 3 : Capacitor value combinations and observed oscillation frequency

| **Capacitor, *C* value** (F) | **Actual Resistor, *R* value** (Ω) | **Actual Frequency, *F*** (Hz) |
|---|---|---|
| 1 nF | 500.00 Ω | 970.874 kHz |
| 4.7 nF | 106.38 Ω | 1.063 MHz |
| 220 pF | 2.40 kΩ | 946.97 kHz |
| 330 pF | 1.515 kΩ | 1.0101 MHz |
| 470 pF | 1.063 kΩ | 1.0638 MHz |

To simplify the process and reduce the variations in oscillation frequency of the sawtooth wave, the wave is derived from a function generator that is able to provide more precise waveform with the desired frequency of 1 Mhz. This function generator will replace the circuit above and will be used throughout the project onwards.

### 3.3.4. PWM Generator Circuit

This circuit as shown in Figure 11 below has been constructed to derive PWM signal for this project's purposes [15].

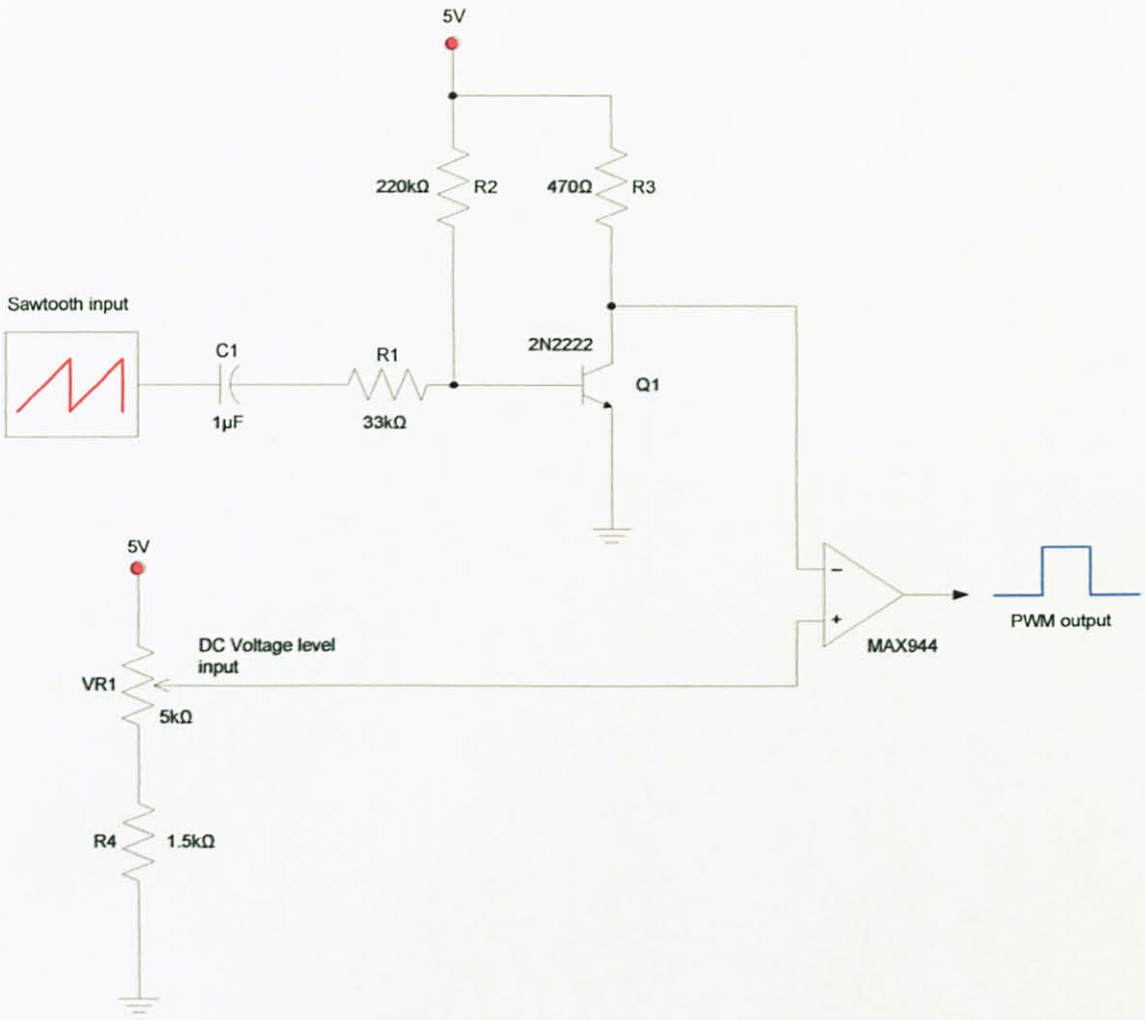



Figure 11: PWM generator circuit schematic

The required PWM signal for this experimentation is 20% - 90% duty cycle at frequency of 1000 kHz (1 MHz). The frequency of the signal is controlled by the frequency of the sawtooth wave input from the function generator. To make sure

that sawtooth signal is fully detected by the reference signal, capacitor $C_1$ and resistor $R_1$ is added to shift up a bit the sawtooth waveform. This is to ensure that this circuit can generate PWM signal with duty ratio from 30% to 70%. The power delivered by the PWM is heavily influenced by the power supplied ($V_{CC}$=5V) to the circuit and PWM duty ratio, $D$ as shown in (10) below:

$$P_{delivered} = V_{CC} \times D \tag{10}$$

The duty ratio can also be expressed by the ON time, $t_{on}$ over the period of the function, $T_s$ as shown in (11):

$$D = \frac{t_{on}}{T_s} = \frac{V_{DC}}{V_{sawtooth}} \tag{11}$$

This circuit amplifies the signal a bit using 2N2222 NPN transistor connected in common emitter configuration. The current gain, β for this transistor is 75 is a ratio between current in collector, $I_C$ and base current $I_B$ (12).

$$\beta = \frac{I_C}{I_B} \tag{12}$$

The determination of resistor at the base, $R_2$ and resistor at the load, $R_3$ are as follows (13) and (14):

$$R_2 = \frac{V_B - V_{BE}}{I_B} \tag{13}$$

$$R_3 = \frac{V_{CC} - V_{CE}}{I_C} \tag{14}$$

It is noted that rectangular pulse is inverse to the sawtooth waveform. However, since this transistor is an inverting amplifier, the PWM signal produced is not inverted. For controlling DC reference signal, voltage divider circuit is used. The amount of DC voltage is related by equation (15) below:

$$V_{DC} = \frac{V_{CC} \times R_4}{VR_1 + R_4} \tag{15}$$

Resistor $R_4$ is connected before ground to prevent DC voltage from falling too much under the bottom edge of the shifted sawtooth signal. By doing this, the whole range of potentiometer *VR1* will have active influence on PWM duty cycle. Hence, PWM duty ratio is set by adjusting the potentiometer *VR1* in the circuit.

# CHAPTER 4

# RESULTS AND DISCUSSIONS

## 4.1 PWM waveform in various frequencies

To determine the frequency operation of this PWM generator circuit, the frequency of sawtooth waveform is varied by adjusting frequency knob of the function generator. The duty cycle is fixed at 50 % to compare the quality of PWM signal generated at different frequency. It is observed that the higher the frequency, the signal is more susceptible to noise as shown in these figures below.

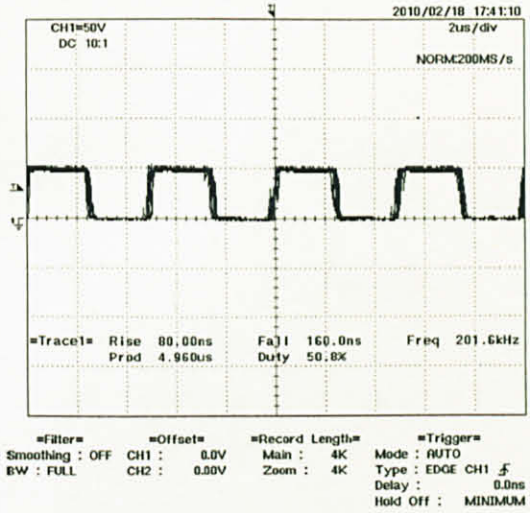



Figure 12 : 50 % duty cycle PWM signal at 200 kHz

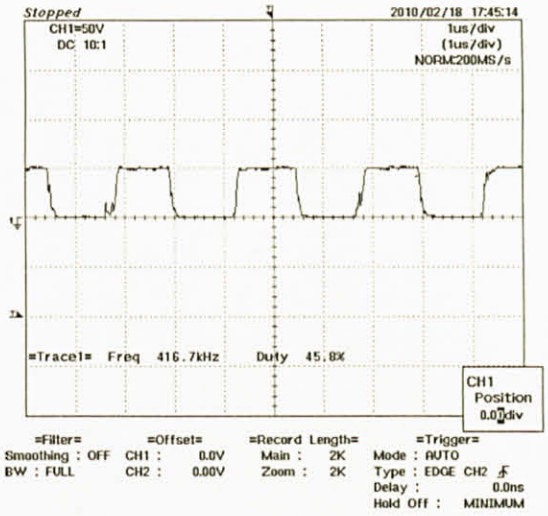



Figure 13 : 50 % duty cycle PWM signal at 400 kHz

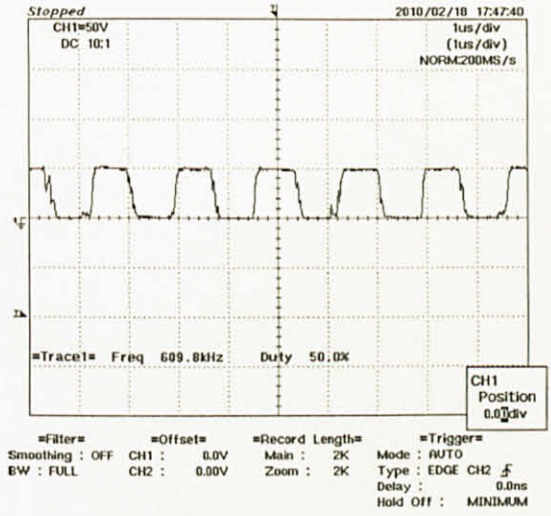



Figure 14 : 50 % duty cycle PWM signal at 600 kHz

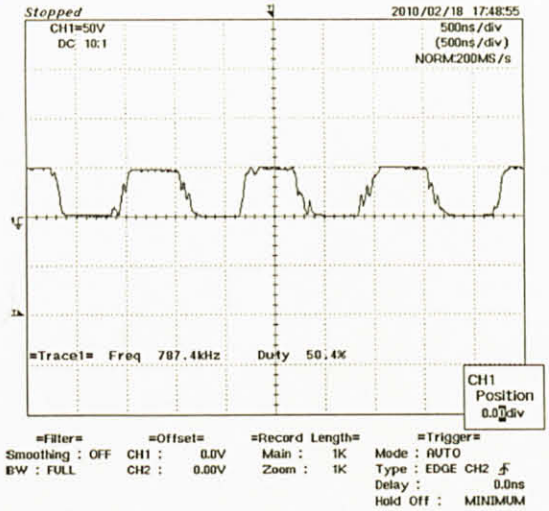



Figure 15 : 50 % duty cycle PWM signal at 800 kHz

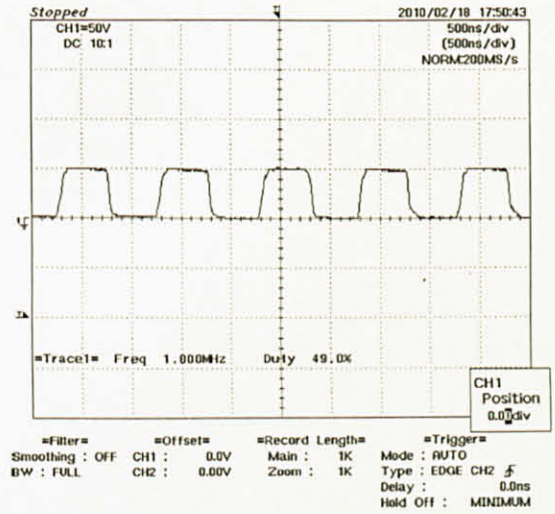



Figure 16 : 50 % duty cycle PWM signal at 1000 kHz (1 MHz)

The frequency of each 50 % duty cycle PWM signal and its respective peak voltages are recorded in Table 4 below:

Table 4 : Frequency and Peak Voltage for 50 % Duty Cycle PWM

| **Frequency, $f$ (kHz)** | **Peak Voltage, $V_{pk}$ (V)** |
|---|---|
| 200 kHz | 50 V |
| 400 kHz | 50 V |
| 600 kHz | 50 V |
| 800 kHz | 50 V |
| 1000 kHz (1 MHz) | 50 V |

From Table 4, it is observed that the circuit is able to generate PWM signal with 50 % duty cycle from frequency of 200 kHz up to 1 MHz and maintaining the same peak voltage. This shows that the generator circuit can maintain the same peak voltage within that frequency range.

## 4.2 PWM waveform of 1 MHz frequency with varying duty cycles

To determine performance of this PWM generator circuit at 1 MHz frequency, the duty cycle is varied by changing the value of DC level voltage. This is done by adjusting the resistance value of potentiometer *VR1* in the circuit. The duty cycle is varied from 20 % to 90 % to compare the quality of PWM signal generated at different duty cycles. It is observed that the PWM signal is less susceptible to noise when the duty cycle is between 30 % to 70 %. The rise time and fall time of each signal is also recorded.

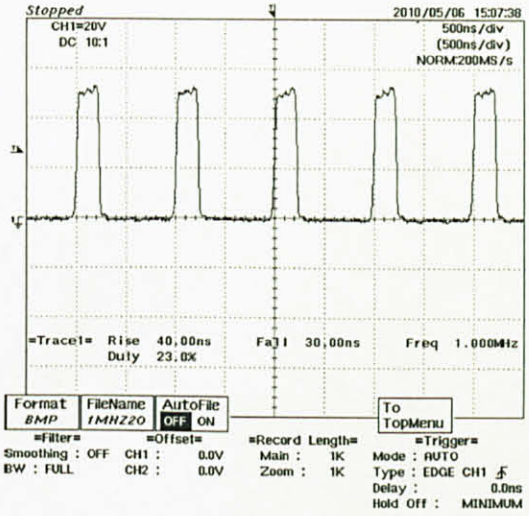



Figure 17 : 1 MHz PWM with 20 % duty cycle

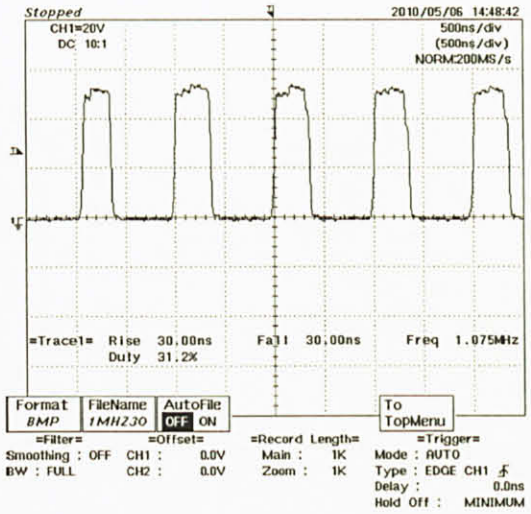



Figure 18 : 1 MHz PWM with 30 % duty cycle

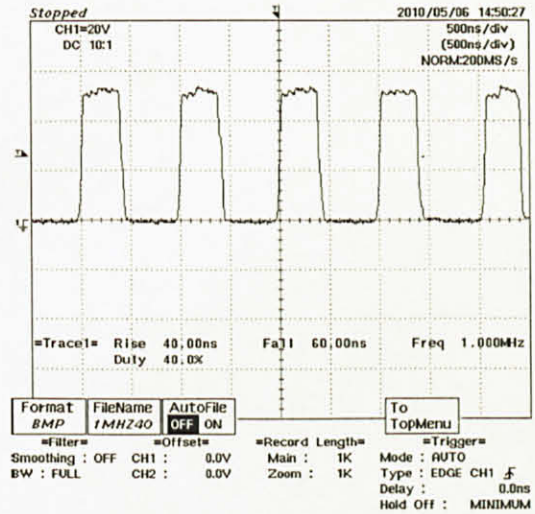



Figure 19 : 1 MHz PWM with 40 % duty cycle

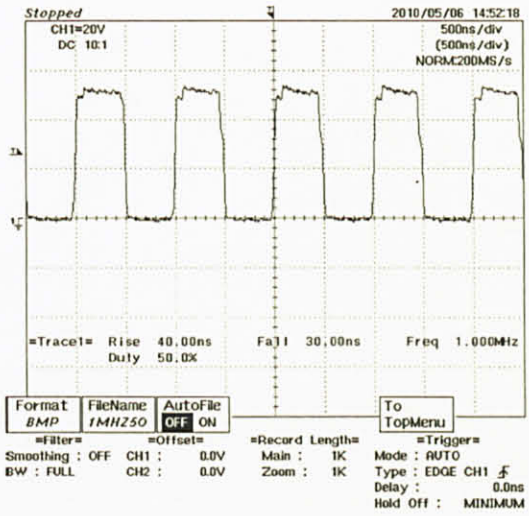



Figure 20 : 1 MHz PWM with 50 % duty cycle

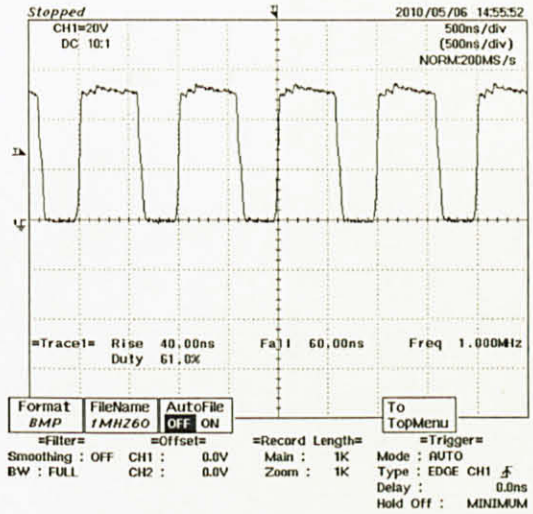



Figure 21 : 1 MHz PWM with 60 % duty cycle

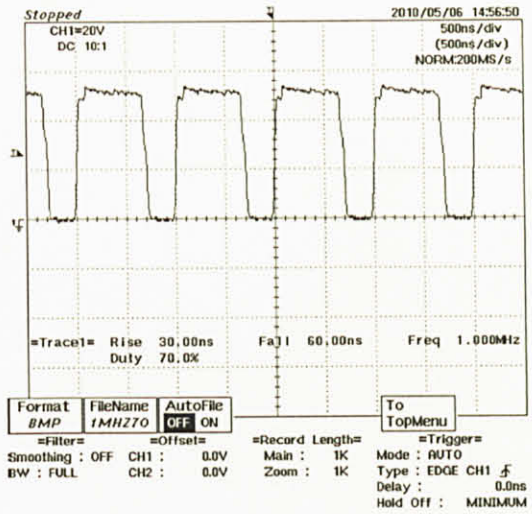



Figure 22 : 1 MHz PWM with 70 % duty cycle

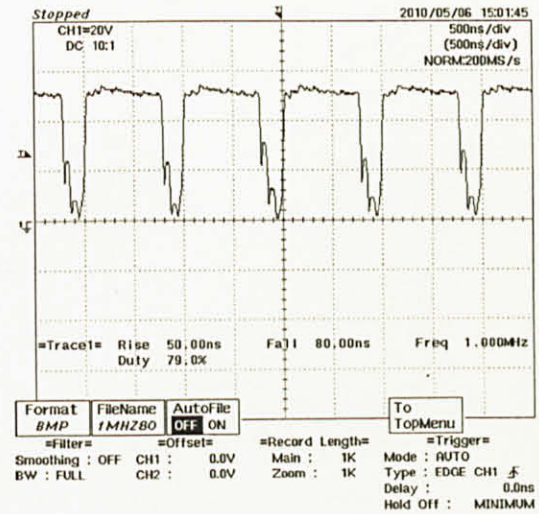



Figure 23 : 1 MHz PWM with 80 % duty cycle

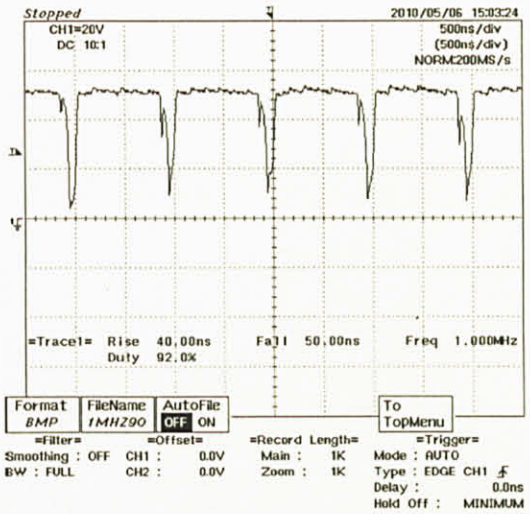



Figure 24 : 1 MHz PWM with 90 % duty cycle

The rise time, fall time and average peak voltage at every duty cycle is recorded in Table 5 below:

Table 5 : Rise time, fall time and average peak voltage of 1 MHz PWM signal at different duty cycles

| **Duty Cycle (%)** | **Rise time, $t_r$ (ns)** | **Fall time, $t_f$ (ns)** | **Average Peak Voltage, $V_{pk}$ (V)** |
|---|---|---|---|
| 20 % | 40.00 ns | 30.00 ns | 48 V |
| 30 % | 30.00 ns | 30.00 ns | 48 V |
| 40 % | 40.00 ns | 60.00 ns | 48 V |
| 50 % | 40.00 ns | 30.00 ns | 48 V |
| 60 % | 40.00 ns | 60.00 ns | 48 V |
| 70 % | 30.00 ns | 60.00 ns | 48 V |
| 80 % | 50.00 ns | 80.00 ns | 48 V |
| 90 % | 40.00 ns | 50.00 ns | 48 V |

From Table 5, the average rise time is 38.75 ns and average fall time is 50.00 ns. However, the average peak voltage is maintained at 48 V in each duty cycles. The best range of operation of this PWM generator circuit is from 30 % to 70 % duty cycle at 1 MHz because the rise time shows little variation in this range.

## 4.3 Resolutions of PWM signals

The resolution of 1 MHz PWM signals at various duty cycles are also recorded as shown in these figures below. The resolution of PWM signals generated is acceptable and the best resolution and low noise combination is observed between 30 % and 70 % duty cycle. This shows that the lower the signal noise, the better the resolution. The signal resolutions are also listed in the Table 6 below.

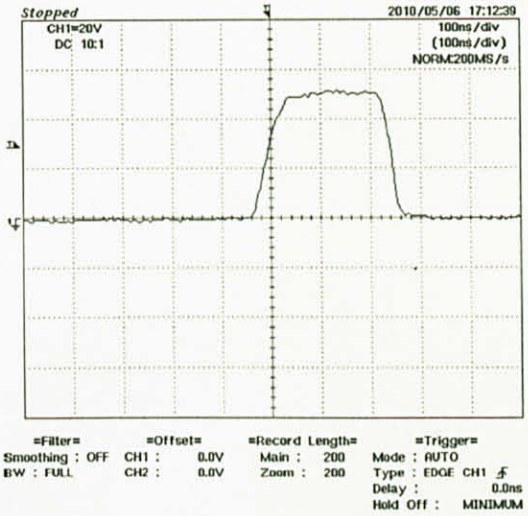



Figure 25: Resolution of 20 % duty cycle 1 MHz PWM

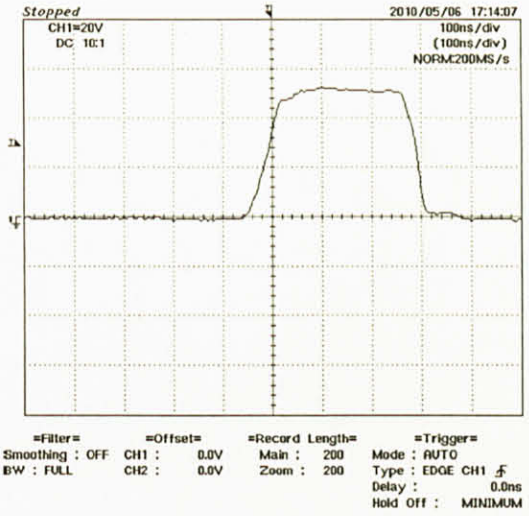



Figure 26 : Resolution of 30 % duty cycle 1 MHz PWM

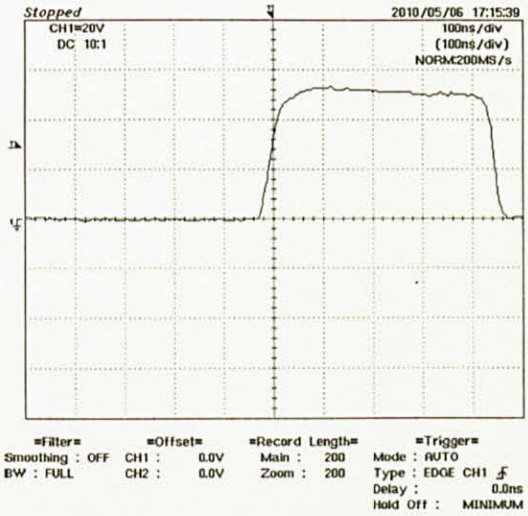



Figure 27 : Resolution of 40 % duty cycle 1 MHz PWM

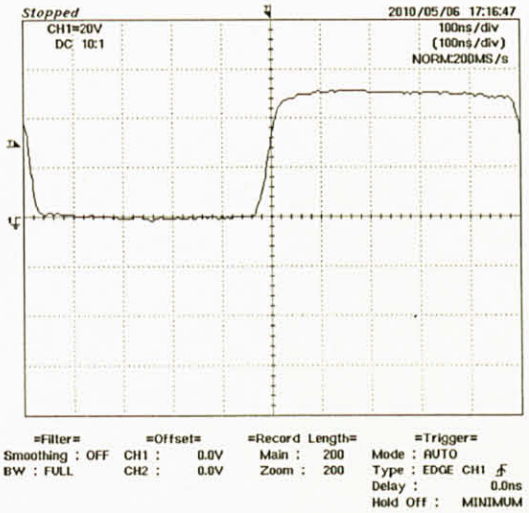



Figure 28 : Resolution of 50 % duty cycle 1 MHz PWM

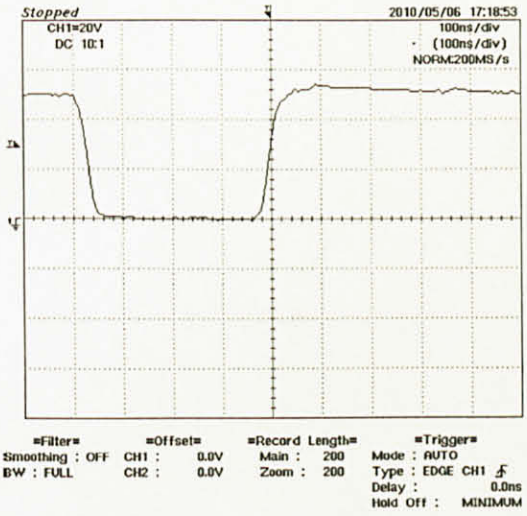



Figure 29 : Resolution of 60 % duty cycle 1 MHz PWM

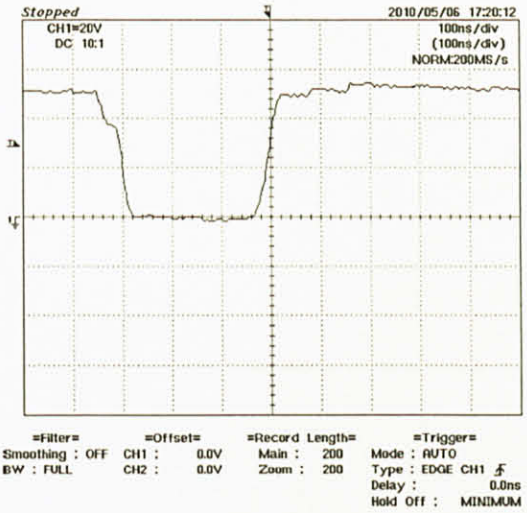



Figure 30 : Resolution of 70 % duty cycle 1 MHz PWM

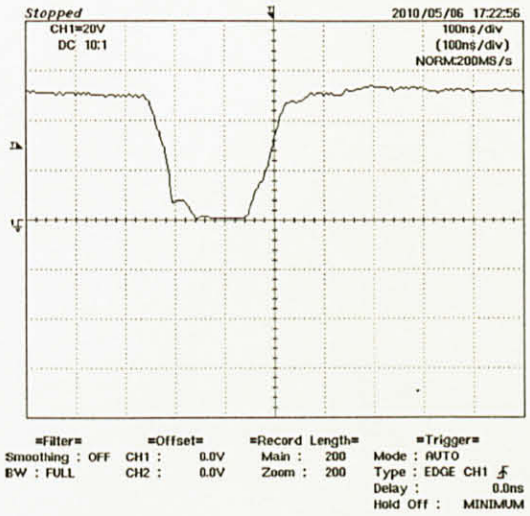



Figure 31 : Resolution of 80 % duty cycle 1 MHz PWM

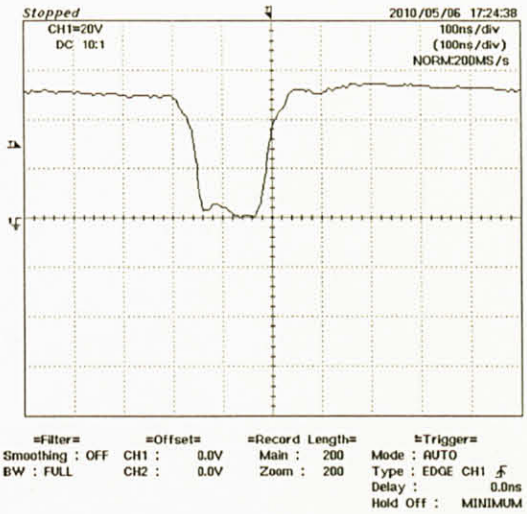



Figure 32 : Resolution of 90 % duty cycle 1 MHz PWM

The PWM signal resolutions are recorded in Table 6 below:

Table 6 : 1 MHz PWM signal resolutions at different duty cycles

| **Duty Cycle** | **Resolution (ns)** |
|---|---|
| 20 % | 0.30 div × 100 ns/div = **30 ns** |
| 30 % | 0.40 div × 100 ns/div = **40 ns** |
| 40 % | 0.20 div × 100 ns/div = **20 ns** |
| 50 % | 0.20 div × 100 ns/div = **20 ns** |
| 60 % | 0.20 div × 100 ns/div = **20 ns** |
| 70 % | 0.18 div × 100 ns/div = **18 ns** |
| 80 % | 0.40 div × 100 ns/div = **40 ns** |
| 90 % | 0.30 div × 100 ns/div = **30 ns** |

The average resolution for 1 MHz PWM signal at different duty cycles as computed from Table 6 is 27.25 ns. From the resolution table, it is observed that from 40 % to 70 % duty cycle, the resolution is the most consistent.

# CHAPTER 5

# CONCLUSION AND RECOMMENDATION

In general, the attempt to generate PWM signal at 1 MHz had been successful with certain limitation. At low frequency, from 200 kHz to 600 kHz, the circuit is less susceptible to noise. It is observed that the circuit is not fully capable of varying the duty cycle very much at 1 MHz. The best PWM that the circuit can generate is in the range of 30 % to 70 % duty cycle at 1 MHz frequency. This capability is sufficient enough for driving power MOSFETs in power electronic converters (buck/boost converter). Very wide duty cycle range is not really needed as the variation of duty cycle is minimal. This is the most demanding application that requires high frequency operation. However, this circuit had at least surpassed the capability of some PWM chips found in the market. PWM chip in the market had two limitations. The first limitation is the operating frequency is not as high as 1 MHz although the range of duty cycle it can operate is high (from 0 % to 100 %). Second limitation is the narrow duty cycle range of PWM available although been able to operate at 1 MHz. This circuit had addressed to this limitation better by providing wider duty cycle range and the ability to operate at high frequency (1 MHz).The comparison can be observed in Table 7 [16][17][18]:

Table 7 : Comparison of different PWM generation methods

| PWM Generation Method | Frequency | Duty Cycle |
|---|---|---|
| PWM Generator Circuit | 0 kHz – 1000 kHz (1 MHz) | 20 % – 90 % |
| TL494 chip | 10 kHz | 0 % – 45 % |
| UC3823A chip | 0.9 MHz – 1.1 MHz | < 100 % |
| SG3526 chip | 1 kHz – 400 kHz | 0 % – 45 % |

The circuit's performance can be better by revising and modifying the original circuit construction. In this circuit, the transistor is biased using fixed-bias. The arrangement is very simple in this type of bias but carries a heavy withdraw [19]. This type of bias is very sensitive to variation in temperature. The DC operating point or quiescent point (Q-point) will change from change in ambient temperature or from current flow within the transistor. The change in Q-point is undesirable because it affects the amplification gain and may result into distortion on the output signal. The suggested biasing for this circuit is by using combination bias [20]. This configuration combines fixed and self bias type of transistor biasing. Using this configuration, the stability of transistor operation can be improved and the limitations on other configurations are overcome. For sensitive high frequency PWM, operation it is recommended to use PWM function generator despite the limited availability of such devices. The use of PWM generator chip is recommended if PWM duty cycle variation is not really needed. However, the circuit used in this project is an average performer due to its wide frequency and duty cycle range. It is suitable for testing purposes where acquiring of those PWM chips and PWM function generator is not possible.

# REFERENCES


[1] Barr, Michael. "Pulse Width Modulation," Embedded Systems Programming, September 2001, pp. 103-104

[2] Li-Jen Liu; Yeong-Chau Kuo; Wen-Chieh Cheng; , "Analog PWM and Digital PWM Controller IC for DC/DC Converters," *Innovative Computing, Information and Control (ICICIC), 2009 Fourth International Conference on* , vol., no., pp.904-907, 7-9 Dec. 2009

[3] Daycounter Inc. (2004) RMS and Average Calculator [Online] Available : http://www.daycounter.com/Calculators/RMS-Calculator.phtml

[4] Malmstadt, Enke and Crouch, Electronics and Instrumentation for Scientists, The Benjamin/Cummings Publishing Company, Inc., 1981, ISBN 0-8053-6917-1, Chapter 5.

[5] T. R. Kuphaldt. (2009, April 5) Positive Feedback in Lessons In Electric Circuits, Volume III – Semiconductors [Online] Available: http://www.allaboutcircuits.com/pdf/ SEMI.pdf

[6] T. R. Kuphaldt. (2009, April 5) Negative Feedback in Lessons In Electric Circuits, Volume III – Semiconductors [Online] Available: http://www.allaboutcircuits.com/pdf/ SEMI.pdf

[7] D.L, Rode; , "Output resistance of the common-emitter amplifier," Electron Devices, IEEE Transactions on , vol.52, no.9, pp. 2004- 2008, Sept. 2005

[8] S. Wayne. (April 2010) The Common Emitter Amplifier [Online] Available: http://www.electronics-tutorials.ws/amplifier/amp_2.html

[9] Takegami, E.; Higuchi, K.; Nakano, K.; Tomioka, S.; Watanabe, K.; , "A method to improve a resolution of digital PWM generator for DC-DC converter control," Computer Aided Control System Design, 2006 IEEE International Conference on Control Applications, 2006 IEEE International Symposium on Intelligent Control, 2006 IEEE , vol., no., pp.3145-3150, 4-6 Oct. 2006

[10] Aubraux. ( - ) All about Rise & Fall Times [Online]. Available: http://www.aubraux.com/design/rise-fall-time.php

[11] Handley, P.G.; Boys, J.T.; , "Resolution corrected modulation: the practical realisation of ideal PWM waveforms," Electric Power Applications, IEE Proceedings B , vol.139, no.4, pp.402-408, Jul 1992

[12] MAX944 High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single Supply Comparators Data Sheet, Maxim Integrated Products, Sunnyvale, CA, March 2009.

[13] PN2222A NPN General Purpose Amplifier Data Sheet, Fairchild Semiconductor Inc., San Jose California, February 2009.

[14] L. Giorgios. ( 2009, July 2) Triangle Wave Generator [Online]. Available: http://pcbheaven.com/circuitpages/Triangle_Wave_Generator/

[15] L. Giorgios. ( 2009, July 3) Voltage Controlled PWM Generator [Online]. Available : http://pcbheaven.com/circuitpages/Voltage_Controlled_PWM_Generator/

[16] TL494 Pulse-Width-Modulation Control Circuits Data Sheet, Texas Instruments, Dallas, TX, February 2005.

[17] UC3823A High-Speed PWM Controller Data Sheet, Texas Instruments, Dallas, TX, November 2008.

[18] SG3526 Pulse Width Modulation Control Circuit Data Sheet, ON Semiconductor, Denver, Colorado, April 2001.

[19] L. Giorgios. ( 2009, February 24) Transistor Theory [Online]. Available : http://pcbheaven.com/wikipages/Transistor_theory/

[20] S. Wayne. (April 2010) The Common Emitter Amplifier [Online] Available: http://www.electronics-tutorials.ws/amplifier/amp_2.html

# APPENDICES

## APPENDIX A

## MAX944 HIGH-SPEED, LOW-POWER, 3V/5V, RAIL-TO-RAIL, SINGLE SUPPLY COMPARATORS DATA SHEET

19-0229; Rev 9; 3/09

MAXIM

# High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators



## General Description

The MAX941/MAX942/MAX944 are single/dual/quad high-speed comparators optimized for systems powered from a 3V or 5V supply. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 80ns, while supply current is only 350µA per comparator.

The input common-mode range of the MAX941/MAX942/MAX944 extends beyond both power-supply rails. The outputs pull to within 0.4V of either supply rail without external pullup circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail.

Internal hysteresis ensures clean output switching, even with slow-moving input signals. The MAX941 features latch enable and device shutdown.

The single MAX941 and dual MAX942 are offered in a tiny µMAX® package. Both the single and dual MAX942 are available in 8-pin DIP and SO packages. The quad MAX944 comes in 14-pin DIP and narrow SO packages.

## Applications

3V/5V Systems

Battery-Powered Systems

Threshold Detectors/Discriminators

Line Receivers

Zero-Crossing Detectors

Sampling Circuits

## Features

- ♦ **Available in µMAX Package for Automotive Applications**
- ♦ **Optimized for 3V and 5V Applications (Operation Down to 2.7V)**
- ♦ **Fast, 80ns Propagation Delay (5mV Overdrive)**
- ♦ **Rail-to-Rail Input Voltage Range**
- ♦ **Low 350µA Supply Current per Comparator**
- ♦ **Low, 1mV Offset Voltage**
- ♦ **Internal Hysteresis for Clean Switching**
- ♦ **Outputs Swing 200mV of Power Rails**
- ♦ **CMOS/TTL-Compatible Outputs**
- ♦ **Output Latch (MAX941 Only)**
- ♦ **Shutdown Function (MAX941 Only)**

## Ordering Information

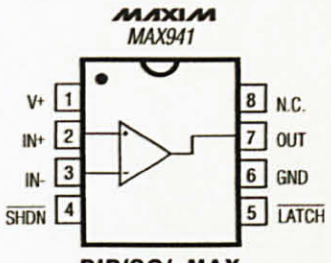
| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX941**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX941CSA | 0°C to +70°C | 8 SO |
| MAX941EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX941ESA | -40°C to +85°C | 8 SO |
| MAX941EUA-T | -40°C to +85°C | 8 µMAX |
| MAX941AUA-T | -40°C to +125°C | 8 µMAX |

***Ordering Information continued at end of data sheet.***

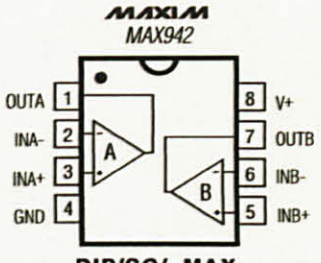
*µMAX is a registered trademark of Maxim Integrated Products, Inc.*

## Pin Configurations

TOP VIEW




DIP/SO/µMAX

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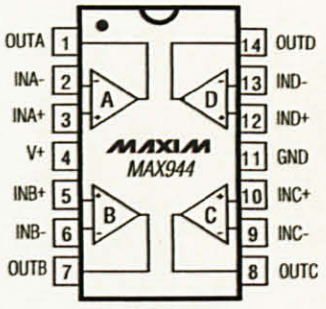



DIP/SO

## ABSOLUTE MAXIMUM RATINGS

Power-Supply Ranges
- Supply Voltage V+ to GND ..... +6.5V
- Differential Input Voltage ..... -0.3V to (V+ + 0.3V)
- Common-Mode Input Voltage ..... -0.3V to (V+ + 0.3V)
- $\overline{LATCH}$ Input (MAX941 only) ..... -0.3V to (V+ + 0.3V)
- $\overline{SHDN}$ Control Input (MAX941 only) ..... -0.3V to (V+ + 0.3V)
- Current Into Input Pins ..... ±20mA

Continuous Power Dissipation ($T_A$ = +70°C)
- 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) ..... 471mW
- 8-Pin µMAX (derate 4.1mW/°C above +70°C) ..... 330mW
- 14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
- 14-Pin SO (derate 8.33mW/°C above +70°C) ..... 667mW

Operating Temperature Ranges
- MAX94_C_ _ ..... 0°C to +70°C
- MAX94_E_ _ ..... -40°C to +85°C
- MAX94_AUA ..... -40°C to +125°C
- MAX942MSA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(V+ = 2.7V to 5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 14)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Positive Supply Voltage | V+ | | | | 2.7 | | 5.5 | V |
| Input Voltage Range | $V_{CMR}$ | (Note 1) | | | -0.2 | | V+ + 0.2 | V |
| Input-Referred Trip Points | $V_{TRIP}$ | $V_{CM}$ = 0 or $V_{CM}$ = V+ (Note 2) | $T_A$ = +25°C | MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA | | 1 | 3 | mV |
| | | | | MAX941_UA/MAX942_UA | | 1 | 4 | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA | | | 4 | mV |
| | | | | MAX941_UA/MAX942_UA | | | 6 | |
| Input Offset Voltage | $V_{OS}$ | $V_{CM}$ = 0 or $V_{CM}$ = V+ (Note 3) | $T_A$ = +25°C | MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA | | 1 | 2 | mV |
| | | | | MAX941_UA/MAX942_UA | | 1 | 3 | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA | | | 3 | mV |
| | | | | MAX941_UA/MAX942_UA | | | 5.5 | |
| Input Bias Current | $I_B$ | $V_{IN}$ = $V_{OS}$, $V_{CM}$ = 0 or $V_{CM}$ = V+ (Note 4) | | MAX94_C | | 150 | 300 | nA |
| | | | | MAX94_E/A, MAX942MSA | | 150 | 400 | |
| Input Offset Current | $I_{OS}$ | $V_{IN}$ = $V_{OS}$, $V_{CM}$ = 0 or V+ | | | | 10 | 150 | nA |
| Input Differential Clamp Voltage | $V_{CLAMP}$ | Force 100µA into IN+, IN- = GND, measure $V_{IN+}$ - $V_{IN-}$, Figure 3 | | | | 2.2 | | V |
| Common-Mode Rejection Ratio | CMRR | (Note 5) | | MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA | | 80 | 300 | µV/V |
| | | | | MAX941_UA/MAX942_UA | | 80 | 800 | |
| Power-Supply Rejection Ratio | PSRR | 2.7V ≤ V+ ≤ 5.5V, $V_{CM}$ = 0V | | MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA | | 80 | 300 | µV/V |
| | | | | MAX941_UA/MAX942_UA | | 80 | 350 | |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 400µA | | | V+ - 0.4 | V+ - 0.2 | | V |
| | | $I_{SOURCE}$ = 4mA | | | V+ - 0.4 | V+ - 0.3 | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 400µA | | | | 0.2 | 0.4 | V |
| | | $I_{SINK}$ = 4mA | | | | 0.3 | 0.4 | |
| Output Leakage Current | $I_{LEAK}$ | (Note 6) | | | | | 1 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.7V to 5.5V, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 14)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current per Comparator | $I_{CC}$ | V+ = 3V | MAX941 | | 380 | 600 | µA |
| | | | MAX942/MAX944 | | 350 | 500 | |
| | | V+ = 5V | MAX941 | | 430 | 700 | |
| | | | MAX942/MAX944 | | 400 | 600 | |
| | | MAX941 only, shutdown mode (V+ = 3V) | | | 12 | 60 | |
| Power Dissipation per Comparator | PD | (Note 7) | MAX941 | | 1.0 | 4.2 | mW |
| | | | MAX942/MAX944 | | 1.0 | 3.6 | |
| Propagation Delay | $t_{PD+}$, $t_{PD-}$ | (Note 8) | MAX94_C | | 80 | 150 | ns |
| | | | MAX94_E/A, MAX942MSA | | 80 | 200 | |
| Differential Propagation Delay | $dt_{PD}$ | (Note 9) | | | 10 | | ns |
| Propagation Delay Skew | | (Note 10) | | | 10 | | ns |
| Logic Input Voltage High | $V_{IH}$ | (Note 11) | | $\frac{V+}{2}$ + 0.4 | $\frac{V+}{2}$ | | V |
| Logic Input Voltage Low | $V_{IL}$ | (Note 11) | | | $\frac{V+}{2}$ | $\frac{V+}{2}$ - 0.4 | V |
| Logic Input Current | $I_{IL}$, $I_{IH}$ | $V_{LOGIC}$ = 0 or V+ (Note 11) | | | 2 | 10 | µA |
| Data-to-Latch Setup Time | $t_S$ | (Note 12) | | | 20 | | ns |
| Latch-to-Data Hold Time | $t_H$ | (Note 12) | | | 30 | | ns |
| Latch Pulse Width | $t_{LPW}$ | MAX941 only | | | 50 | | ns |
| Latch Propagation Delay | $t_{LPD}$ | MAX941 only | | | 70 | | ns |
| Shutdown Time | | (Note 13) | | | 3 | | µs |
| Shutdown Disable Time | | (Note 13) | | | 10 | | µs |

**Note 1:** Inferred from the CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.

**Note 2:** The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone (see Figure 1).

**Note 3:** $V_{OS}$ is defined as the center of the input-referred hysteresis zone (see Figure 1).

**Note 4:** The polarity of $I_B$ reverses direction as $V_{CM}$ approaches either supply rail. See *Typical Operating Characteristics* for more detail.

**Note 5:** Specified over the full common-mode range ($V_{CMR}$).

**Note 6:** Applies to the MAX941 only when in shutdown mode. Specification is for current flowing into or out of the output pin for $V_{OUT}$ driven to any voltage from V+ to GND.

**Note 7:** Typical power dissipation specified with V+ = 3V; maximum with V+ = 5.5V.

**Note 8:** Parameter is guaranteed by design and specified with $V_{OD}$ = 5mV and $C_{LOAD}$ = 15pF in parallel with 400µA of sink or source current. $V_{OS}$ is added to the overdrive voltage for low values of overdrive (see Figure 2).

**Note 9:** Specified between any two channels in the MAX942/MAX944.

**Note 10:** Specified as the difference between $t_{PD+}$ and $t_{PD-}$ for any one comparator.

**Note 11:** Applies to the MAX941 only for both $\overline{SHDN}$ and $\overline{LATCH}$ pins.

**Note 12:** Applies to the MAX941 only. Comparator is active with $\overline{LATCH}$ pin driven high and is latched with $\overline{LATCH}$ pin driven low (see Figure 2).

**Note 13:** Applicable to the MAX941 only. Comparator is active with $\overline{SHDN}$ pin driven high and is in shutdown with $\overline{SHDN}$ pin driven low. Shutdown disable time is the delay when $\overline{SHDN}$ is driven high to the time the output is valid.

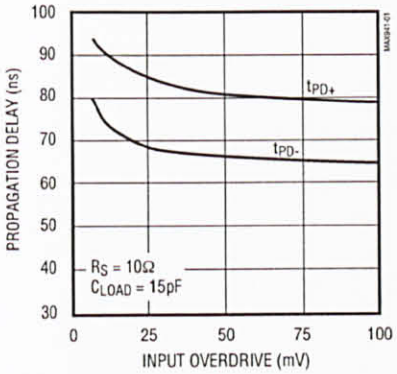
**Note 14:** The MAX941_UA and MAX942_UA are 100% production tested at $T_A$ = +25°C. Specifications over temperature are guaranteed by design.

# High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

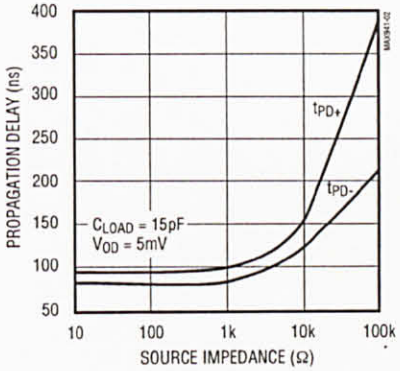
## Typical Operating Characteristics

(V+ = 3.0V, $T_A$ = +25°C, unless otherwise noted.)

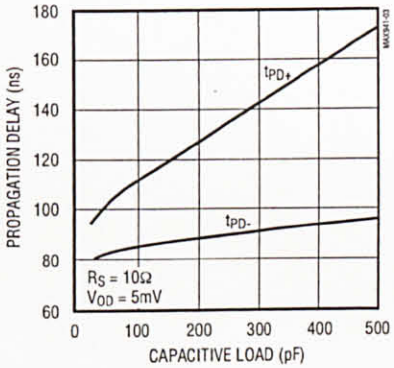
**PROPAGATION DELAY vs. INPUT OVERDRIVE**



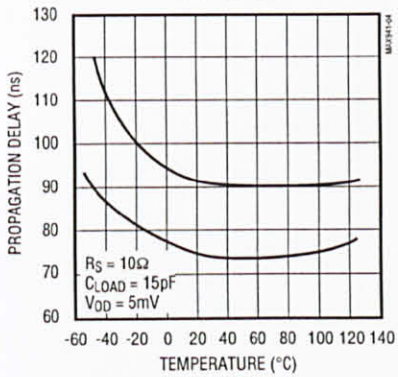

**PROPAGATION DELAY vs. SOURCE IMPEDANCE**



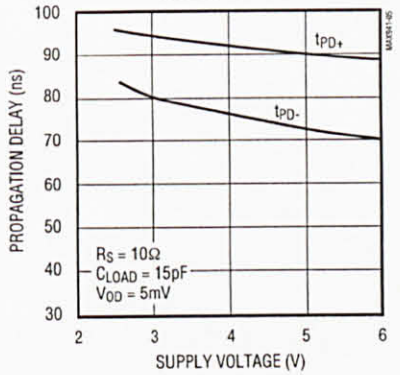

**PROPAGATION DELAY vs. CAPACITIVE LOAD**



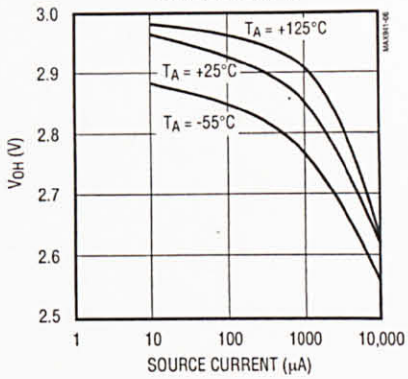

**PROPAGATION DELAY vs. TEMPERATURE**



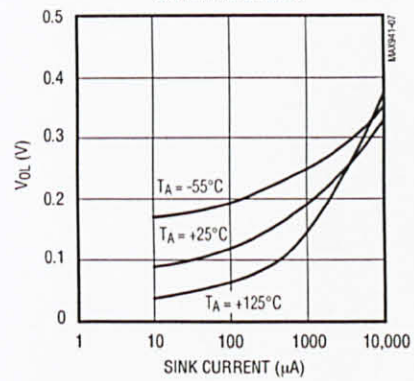

**PROPAGATION DELAY vs. SUPPLY VOLTAGE**



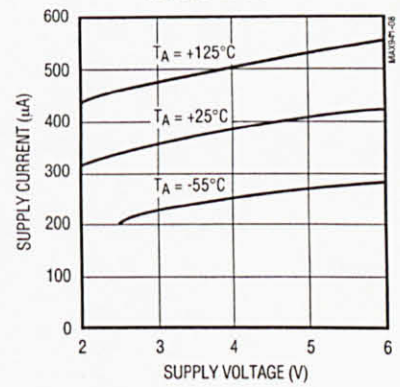

**OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT**



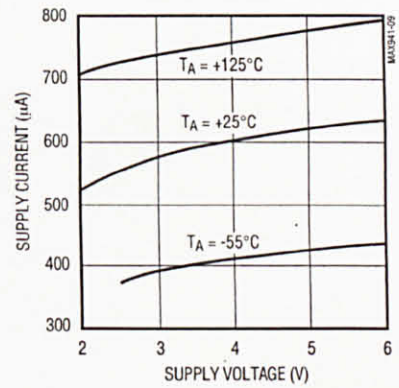

**OUTPUT LOW VOLTAGE vs. SINK CURRENT**




**MAX941 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE**




**MAX942 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE**

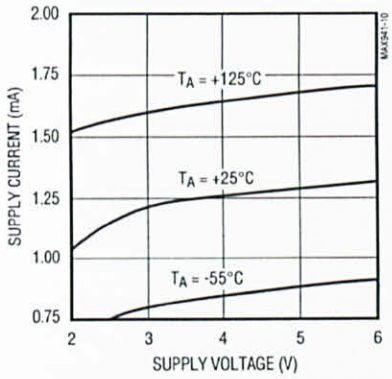


# High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

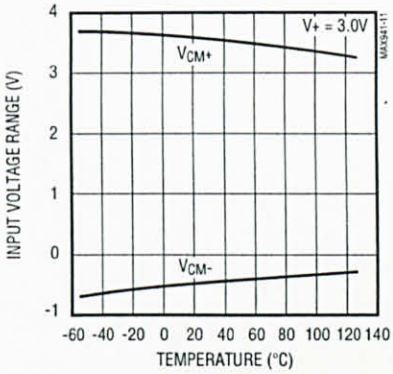
## Typical Operating Characteristics (continued)

(V+ = 3.0V, $T_A$ = +25°C, unless otherwise noted.)

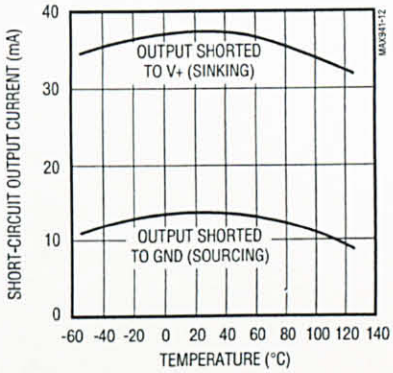
**MAX944 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE**



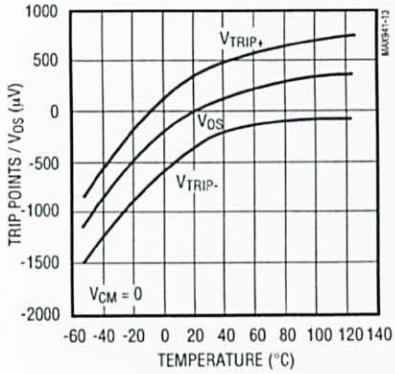

**INPUT VOLTAGE RANGE vs. TEMPERATURE**



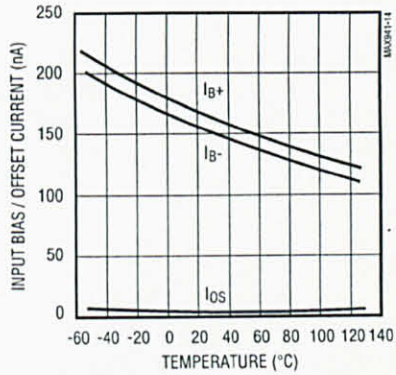

**SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE**



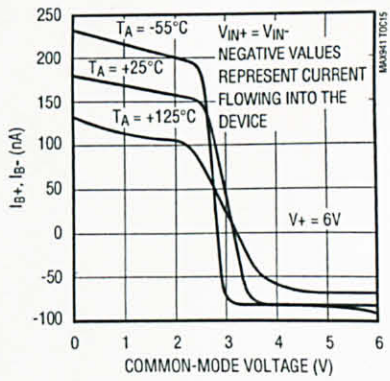

**VOLTAGE TRIP POINTS/INPUT OFFSET VOLTAGE vs. TEMPERATURE**



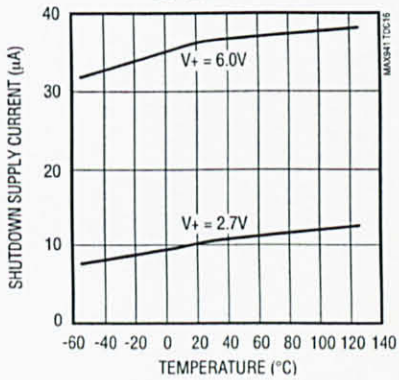

**INPUT BIAS CURRENT/INPUT OFFSET CURRENT vs. TEMPERATURE**



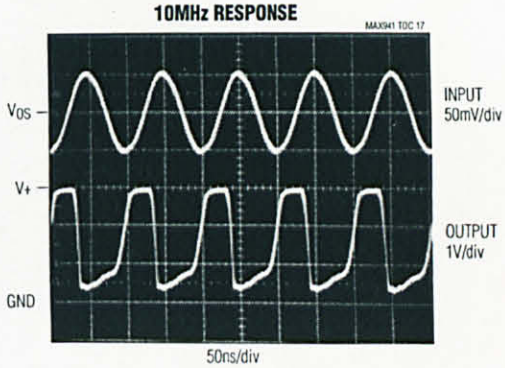

**INPUT BIAS CURRENT ($I_{B+}$, $I_{B-}$) vs. COMMON-MODE VOLTAGE**




**MAX941 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE**



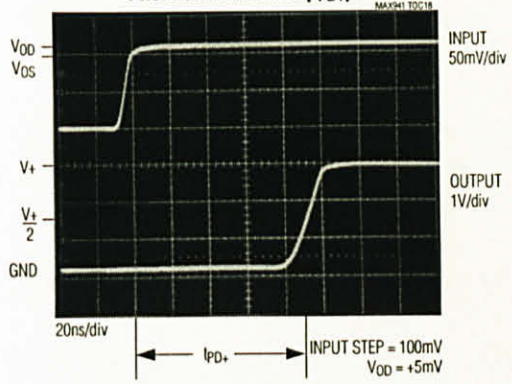

**10MHz RESPONSE**



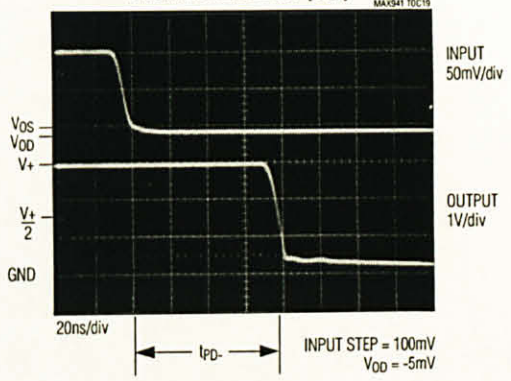
## Typical Operating Characteristics (continued)

(V+ = 3.0V, $T_A$ = +25°C, unless otherwise noted.)

**PROPAGATION DELAY ($t_{PD+}$)**




**PROPAGATION DELAY ($t_{PD-}$)**




## Pin Description

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| MAX941 | MAX942 | MAX944 | | |
| — | 1 | 1 | OUTA | Comparator A Output |
| — | 2 | 2 | INA- | Comparator A Inverting Input |
| — | 3 | 3 | INA+ | Comparator A Noninverting Input |
| 1 | 8 | 4 | V+ | Positive Supply (V+ to GND must be ≤ 6.5V) |
| — | 5 | 5 | INB+ | Comparator B Noninverting Input |
| — | 6 | 6 | INB- | Comparator B Inverting Input |
| — | 7 | 7 | OUTB | Comparator B Output |
| — | — | 8 | OUTC | Comparator C Output |
| — | — | 9 | INC- | Comparator C Inverting Input |
| — | — | 10 | INC+ | Comparator C Noninverting Input |
| 6 | 4 | 11 | GND | Ground |
| — | — | 12 | IND+ | Comparator D Noninverting Input |
| — | — | 13 | IND- | Comparator D Inverting Input |
| — | — | 14 | OUTD | Comparator D Output |
| 2 | — | — | IN+ | Noninverting Input |
| 3 | — | — | IN- | Inverting Input |
| 4 | — | — | $\overline{SHDN}$ | Shutdown: MAX941 is active when $\overline{SHDN}$ is driven high; MAX941 is in shutdown when $\overline{SHDN}$ is driven low. |
| 5 | — | — | $\overline{LATCH}$ | The output is latched when $\overline{LATCH}$ is low. The latch is transparent when $\overline{LATCH}$ is high. |
| 7 | — | — | OUT | Comparator Output |
| 8 | — | — | N.C. | No Connection. Not internally connected. |

# High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

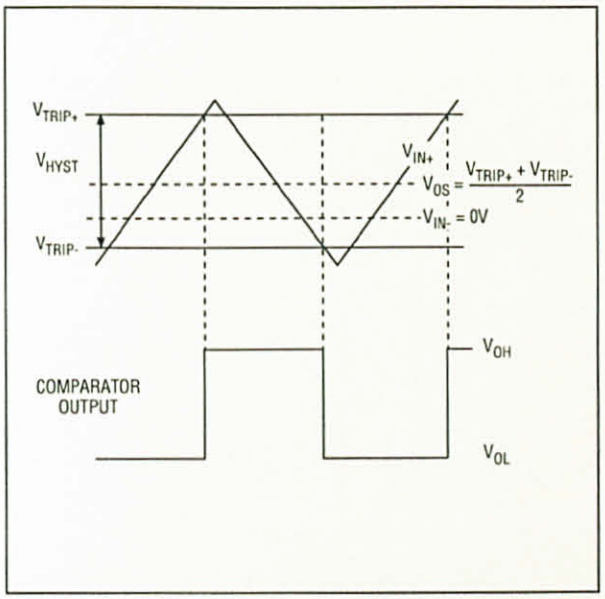



*Figure 1. Input and Output Waveform, Noninverting Input Varied*

## Detailed Description

The MAX941/MAX942/MAX944 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are guaranteed to pull within 0.4V of either supply rail without external pullup or pulldown circuitry. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment. The MAX941/MAX942/MAX944 interface directly to CMOS and TTL logic.

### Timing

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the MAX941/MAX942/MAX944 have internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX941/MAX942/MAX944's fixed internal hysteresis eliminates these resistors and the equations needed to determine appropriate values.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX941 includes an internal latch that allows storage of comparison results. The $\overline{LATCH}$ pin has a high input impedance. If $\overline{LATCH}$ is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when $\overline{LATCH}$ is pulled low. All timing constraints must be met when using the latch function (Figure 2).

### Shutdown Mode (MAX941 Only)

The MAX941 shuts down when $\overline{SHDN}$ is low. When shut down, the supply current drops to less than 60µA, and the three-state output becomes high impedance. The $\overline{SHDN}$ pin has a high input impedance. Connect $\overline{SHDN}$ to V+ for normal operation. Exit shutdown with $\overline{LATCH}$ high; otherwise, the output will be indeterminate.

### Input Stage Circuitry

The MAX941/MAX942/MAX944 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two back-to-back diodes between IN+ and IN- as well as two 4.1kΩ resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to be no more than $2V_F$, where $V_F$ is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding $2V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input Current} = \frac{(IN+ - IN-) - 2V_F}{2 \times 4.1k\Omega}$$

Input current with large differential input voltages should not be confused with input bias current ($I_B$). As long as the differential input voltage is less than $2V_F$, this input current is equal to $I_B$. The protection circuitry also allows for the input common-mode range of the MAX941/MAX942/MAX944 to extend beyond both power-supply rails. The output is in the correct logic state if one or both inputs are within the common-mode range.

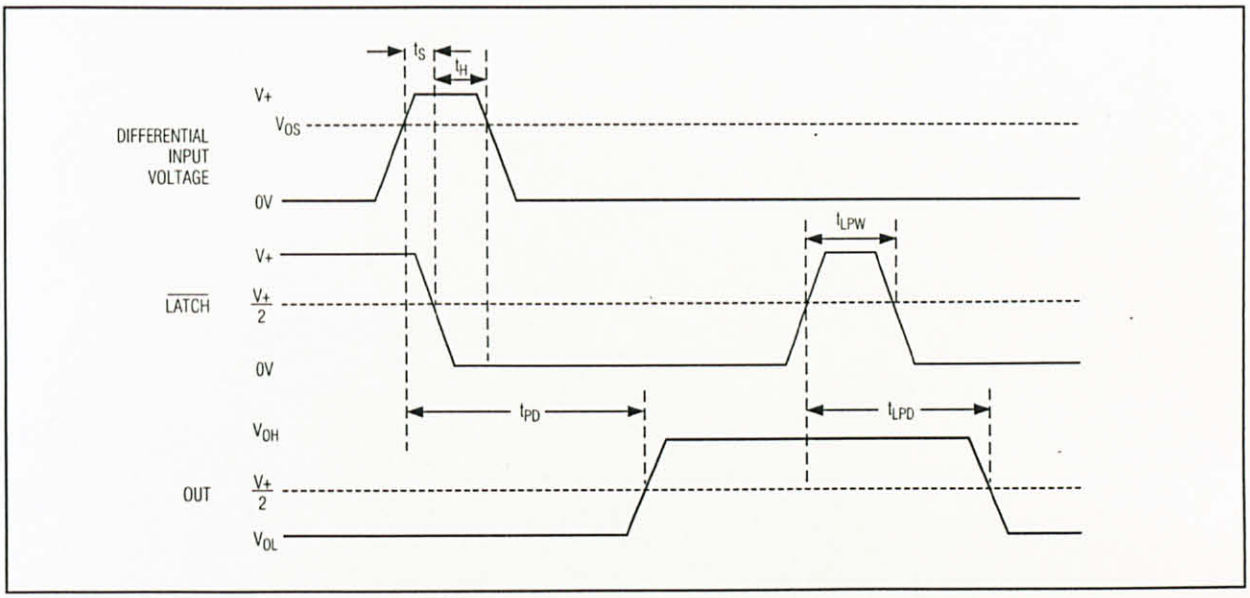



*Figure 2. MAX941 Timing Diagram with Latch Operator*

### Output Stage Circuitry

The MAX941/MAX942/MAX944 contain a current-driven output stage as shown in Figure 4. During an output transition, $I_{SOURCE}$ or $I_{SINK}$ is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches $V_{OH}$ or $V_{OL}$, the source or sink current decreases to a small value, capable of maintaining the $V_{OH}$ or $V_{OL}$ static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noise-sensitive applications where fast edges may cause interference.

## Applications Information

### Circuit Layout and Bypassing

The high gain bandwidth of the MAX941/MAX942/MAX944 requires design precautions to realize the comparators' full high-speed capability. The recommended precautions are:

1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V+ as possible.
3) Pay close attention to the decoupling capacitor's bandwidth, keeping leads short.
4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
5) Solder the device directly to the printed circuit board instead of using a socket.

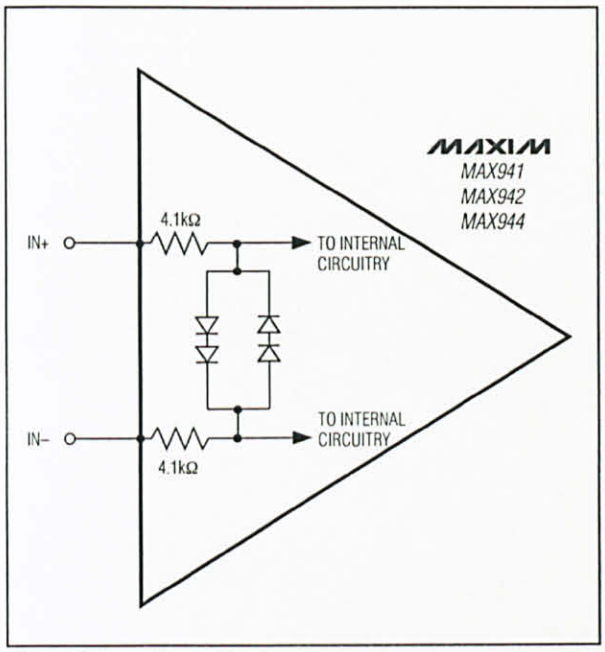



Figure 3. Input Stage Circuitry

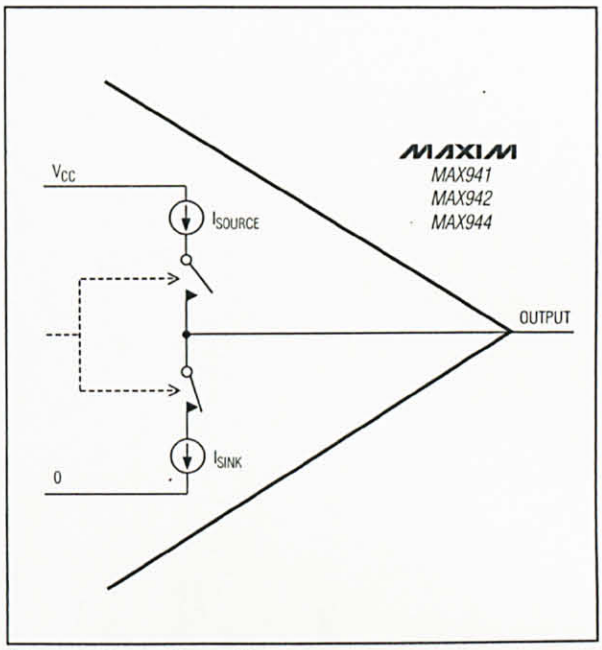



Figure 4. Output Stage Circuitry

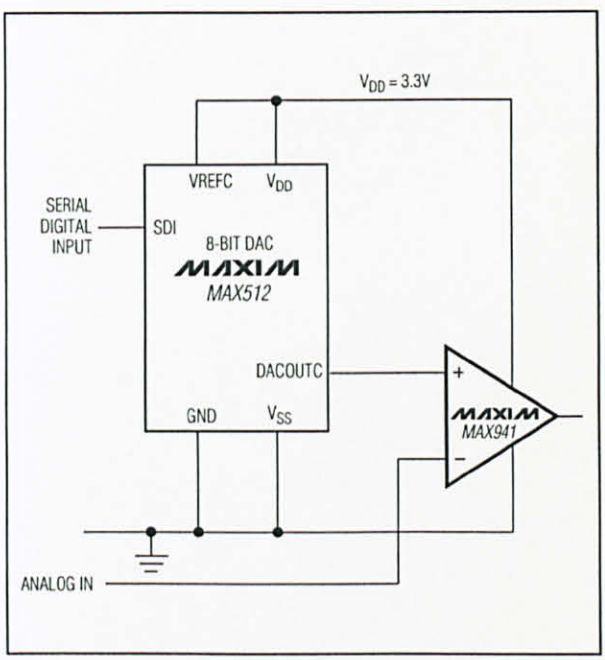



Figure 5. 3.3V Digitally Controlled Threshold Detector

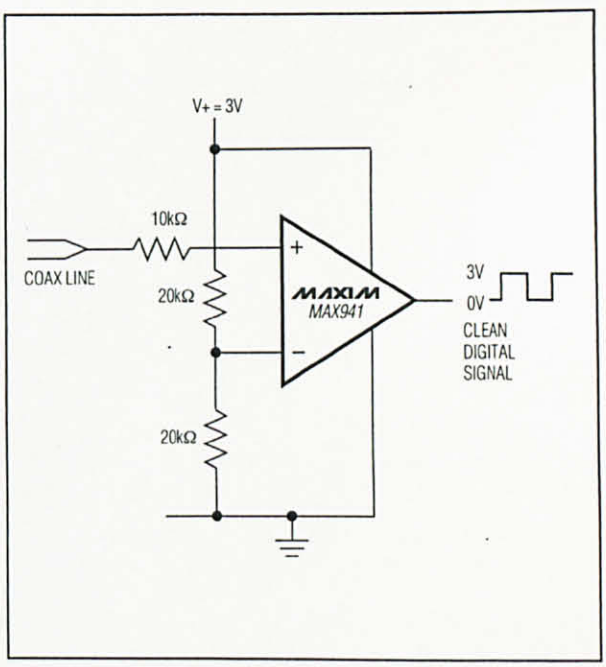



Figure 6. Line Transceiver Application

## Ordering Information (continued)

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX942**MSA/PR | -55°C to +125°C | 8 SO |
| MAX942CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX942CSA | 0°C to +70°C | 8 SO |
| MAX942EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX942ESA | -40°C to +85°C | 8 SO |
| MAX942EUA-T | -40°C to +85°C | 8 µMAX |
| MAX942AUA-T | -40°C to +125°C | 8 µMAX |
| **MAX944**CPD | 0°C to +70°C | 14 Plastic DIP |
| MAX944CSD | 0°C to +70°C | 14 SO |
| MAX944EPD | -40°C to +85°C | 14 Plastic DIP |
| MAX944ESD | -40°C to +85°C | 14 SO |

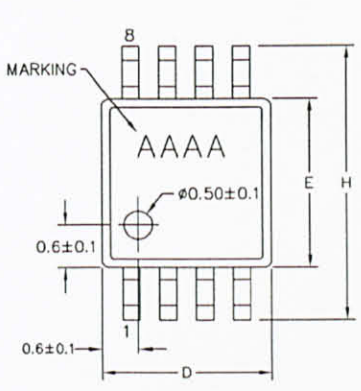
## Chip Information

PROCESS: BiPOLAR

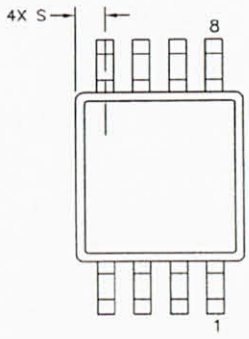
## Package Information

(For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.)

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 8 µMAX | U8-1 | 21-0036 |
| 8 Plastic DIP | P8-1 | 21-0043 |
| 8 SO | S8-2 | 21-0041 |
| 14 Plastic DIP | P14-3 | 21-0043 |
| 14 SO | S14-1 | 21-0041 |

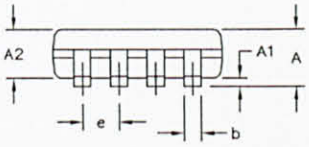



TOP VIEW

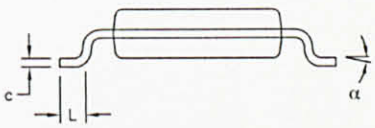



BOTTOM VIEW

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | – | 0.043 | – | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 |
| b | 0.010 | 0.014 | 0.25 | 0.36 |
| c | 0.005 | 0.007 | 0.13 | 0.18 |
| D | 0.114 | 0.122 | 2.90 | 3.10 |
| e | 0.0256 BSC | | 0.65 BSC | |
| E | 0.114 | 0.122 | 2.90 | 3.10 |
| H | 0.188 | 0.198 | 4.78 | 5.03 |
| L | 0.016 | 0.026 | 0.41 | 0.66 |
| α | 0° | 6° | 0° | 6° |
| S | 0.0207 BSC | | 0.5250 BSC | |
| PKG. CODES: U8-1; U8-3; U8CN-1 | | | | |




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO-187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

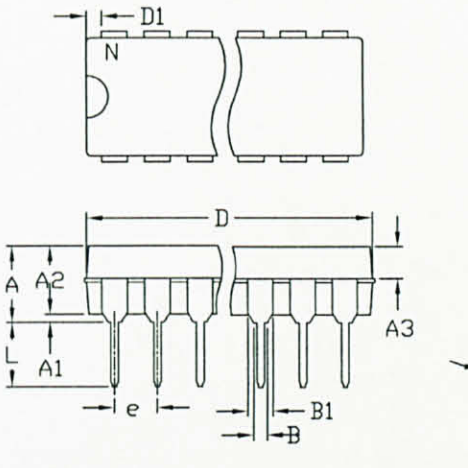
TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0036 | L | 1/1 |

## Package Information (continued)

(For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.)

PDIPN.EPS




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.180 | --- | 4.572 |
| A1 | 0.015 | --- | 0.38 | --- |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.015 | 0.022 | 0.381 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.014 | 0.2 | 0.355 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 BSC. | | 2.54 BSC. | |
| eA | 0.300 BSC. | | 7.62 BSC. | |
| eB | 0.400 BSC. | | 10.16 BSC. | |
| L | 0.115 | 0.150 | 2.921 | 3.81 |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | MS001 |
| D | 0.348 | 0.390 | 8.84 | 9.91 | 8 | AB |
| D | 0.735 | 0.765 | 18.67 | 19.43 | 14 | AC |
| D | 0.745 | 0.765 | 18.92 | 19.43 | 16 | AA |
| D | 0.885 | 0.915 | 22.48 | 23.24 | 18 | AD |
| D | 1.015 | 1.045 | 25.78 | 26.54 | 20 | AE |
| D | 1.14 | 1.265 | 28,96 | 32.13 | 24 | AF |
| D | 1.360 | 1.380 | 34.54 | 35.05 | 28 | *5 |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM — PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 D (DOCUMENT CONTROL NUMBER / REV)

## Package Information (continued)

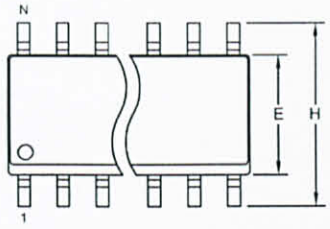
(For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.)

SOICN .EPS

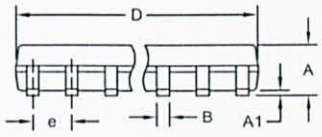
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

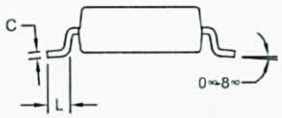
| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | N | MS012 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |




TOP VIEW




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0041 | B | 1/1 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 8 | 12/08 | Added SO package diagram and removed transistor count | 10 |
| 9 | 3/09 | Corrected *Ordering Information* for MAX944ESD | 10 |

# APPENDIX B

## PN2222A NPN GENERAL PURPOSE AMPLIFIER DATA SHEET

FAIRCHILD
SEMICONDUCTOR®

February 2009

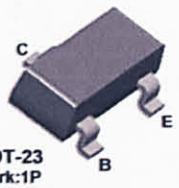
# PN2222A/MMBT2222A/PZT2222A
# NPN General Purpose Amplifier

- This device is for use as a medium power amplifier and switch requiring collector currents up to 500mA.
- Sourced from process 19.

PN2222A

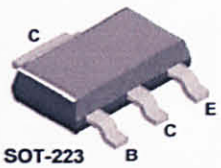

TO-92

MMBT2222A




SOT-23
Mark:1P

PZT2222A




SOT-223

## Absolute Maximum Ratings * $T_a$ = 25×C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{CEO}$ | Collector-Emitter Voltage | 40 | V |
| $V_{CBO}$ | Collector-Base Voltage | 75 | V |
| $V_{EBO}$ | Emitter-Base Voltage | 6.0 | V |
| $I_C$ | Collector Current | 1.0 | A |
| $T_{STG}$ | Operating and Storage Junction Temperature Range | - 55 ~ 150 | °C |

* This ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

**NOTES:**

1) These rating are based on a maximum junction temperature of 150 degrees C.

2) These are steady limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

## Thermal Characteristics $T_a$ = 25°C unless otherwise noted

| Symbol | Parameter | Max. | | | Units |
|---|---|---|---|---|---|
| | | PN2222A | *MMBT2222A | **PZT2222A | |
| $P_D$ | Total Device Dissipation<br>Derate above 25°C | 625<br>5.0 | 350<br>2.8 | 1,000<br>8.0 | mW<br>mW/°C |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 83.3 | | | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 200 | 357 | 125 | °C/W |

* Device mounted on FR-4 PCB 1.6" × 1.6" × 0.06".

** Device mounted on FR-4 PCB 36mm × 18mm × 1.5mm; mounting pad for the collector lead min. 6cm$^2$.

## Electrical Characteristics $T_a$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| **Off Characteristics** | | | | | |
| $BV_{(BR)CEO}$ | Collector-Emitter Breakdown Voltage * | $I_C$ = 10mA, $I_B$ = 0 | 40 | | V |
| $BV_{(BR)CBO}$ | Collector-Base Breakdown Voltage | $I_C$ = 10μA, $I_E$ = 0 | 75 | | V |
| $BV_{(BR)EBO}$ | Emitter-Base Breakdown Voltage | $I_E$ = 10μA, $I_C$ = 0 | 6.0 | | V |
| $I_{CEX}$ | Collector Cutoff Current | $V_{CE}$ = 60V, $V_{EB(off)}$ = 3.0V | | 10 | nA |
| $I_{CBO}$ | Collector Cutoff Current | $V_{CB}$ = 60V, $I_E$ = 0<br>$V_{CB}$ = 60V, $I_E$ = 0, $T_a$ = 125°C | | 0.01<br>10 | μA<br>μA |
| $I_{EBO}$ | Emitter Cutoff Current | $V_{EB}$ = 3.0V, $I_C$ = 0 | | 10 | nA |
| $I_{BL}$ | Base Cutoff Current | $V_{CE}$ = 60V, $V_{EB(off)}$ = 3.0V | | 20 | nA |
| **On Characteristics** | | | | | |
| $h_{FE}$ | DC Current Gain | $I_C$ = 0.1mA, $V_{CE}$ = 10V<br>$I_C$ = 1.0mA, $V_{CE}$ = 10V<br>$I_C$ = 10mA, $V_{CE}$ = 10V<br>$I_C$ = 10mA, $V_{CE}$ = 10V, $T_a$ = -55°C<br>$I_C$ = 150mA, $V_{CE}$ = 10V *<br>$I_C$ = 150mA, $V_{CE}$ = 10V *<br>$I_C$ = 500mA, $V_{CE}$ = 10V * | 35<br>50<br>75<br>35<br>100<br>50<br>40 | <br><br><br><br>300<br><br> | |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage * | $I_C$ = 150mA, $V_{CE}$ = 10V<br>$I_C$ = 500mA, $V_{CE}$ = 10V | | 0.3<br>1.0 | V<br>V |
| $V_{BE(sat)}$ | Base-Emitter Saturation Voltage * | $I_C$ = 150mA, $V_{CE}$ = 10V<br>$I_C$ = 500mA, $V_{CE}$ = 10V | 0.6 | 1.2<br>2.0 | V<br>V |
| **Small Signal Characteristics** | | | | | |
| $f_T$ | Current Gain Bandwidth Product | $I_C$ = 20mA, $V_{CE}$ = 20V, f = 100MHz | 300 | | MHz |
| $C_{obo}$ | Output Capacitance | $V_{CB}$ = 10V, $I_E$ = 0, f = 1MHz | | 8.0 | pF |
| $C_{ibo}$ | Input Capacitance | $V_{EB}$ = 0.5V, $I_C$ = 0, f = 1MHz | | 25 | pF |
| $rb'C_c$ | Collector Base Time Constant | $I_C$ = 20mA, $V_{CB}$ = 20V, f = 31.8MHz | | 150 | pS |
| NF | Noise Figure | $I_C$ = 100μA, $V_{CE}$ = 10V,<br>$R_S$ = 1.0KΩ, f = 1.0KHz | | 4.0 | dB |
| $Re(h_{ie})$ | Real Part of Common-Emitter High Frequency Input Impedance | $I_C$ = 20mA, $V_{CE}$ = 20V, f = 300MHz | | 60 | Ω |
| **Switching Characteristics** | | | | | |
| $t_d$ | Delay Time | $V_{CC}$ = 30V, $V_{EB(off)}$ = 0.5V,<br>$I_C$ = 150mA, $I_{B1}$ = 15mA | | 10 | ns |
| $t_r$ | Rise Time | | | 25 | ns |
| $t_s$ | Storage Time | $V_{CC}$ = 30V, $I_C$ = 150mA,<br>$I_{B1}$ = $I_{B2}$ = 15mA | | 225 | ns |
| $t_f$ | Fall Time | | | 60 | ns |

* Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%

## Typical Characteristics

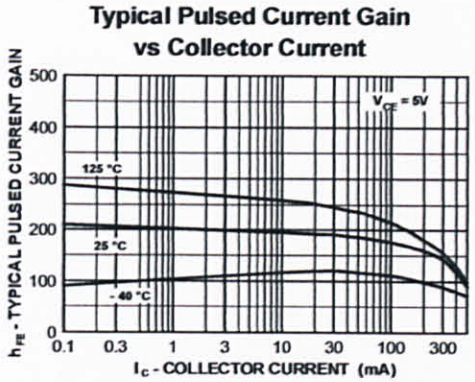



Figure 1. Typical Pulsed Current Gain vs Collector Current

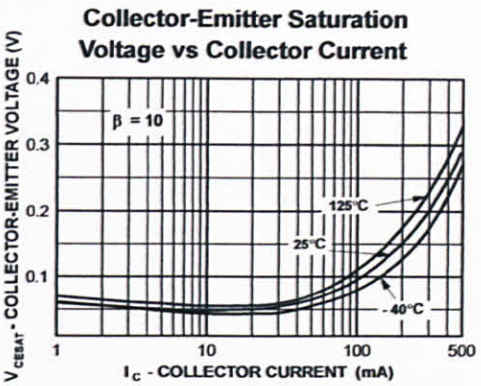



Figure 2. Collector-Emitter Saturation Voltage vs Collector Current

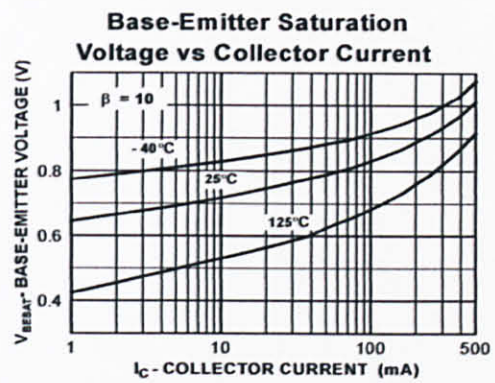



Figure 3. Base-Emitter Saturation Voltage vs Collector Current

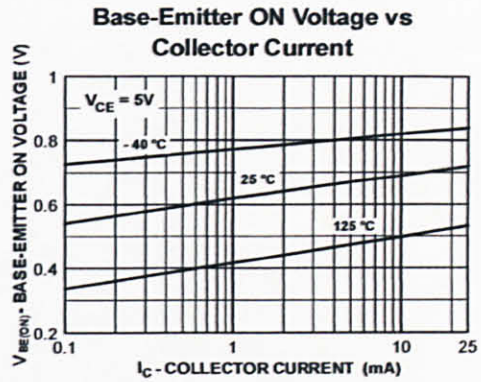



Figure 4. Base-Emitter On Voltage vs Collector Current

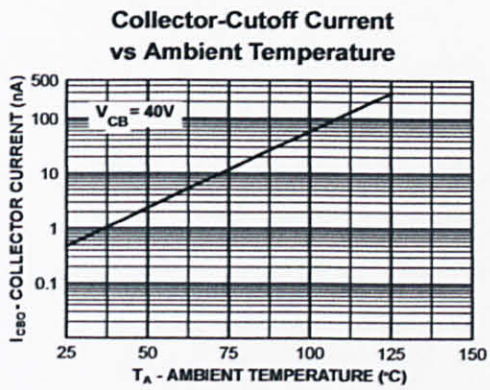



Figure 5. Collector Cutoff Current vs Ambient Temperature

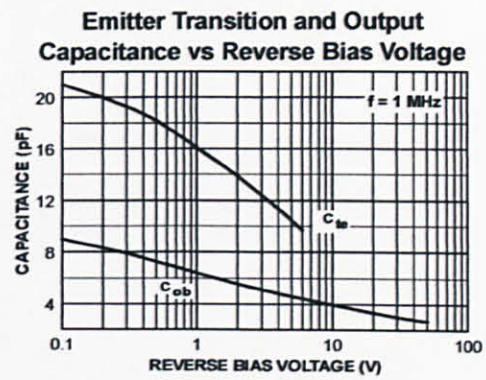



Figure 6. Emitter Transition and Output Capacitance vs Reverse Bias Voltage

# Typical Characteristics

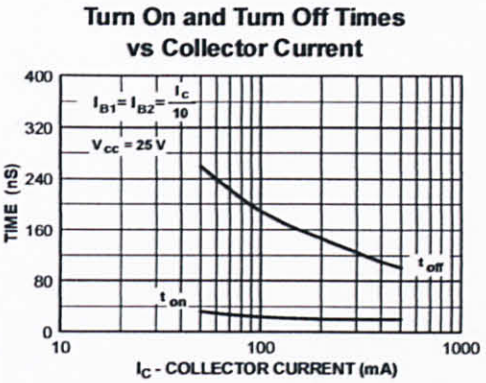



Figure 1. Turn On and Turn Off Times vs Collector Current

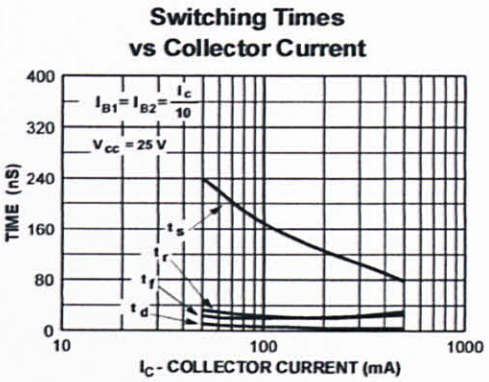



Figure 2. Switching Times vs Collector Current

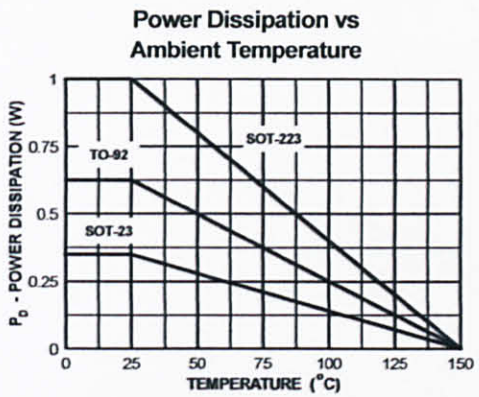



Figure 3. Power Dissipation vs Ambient Temperature

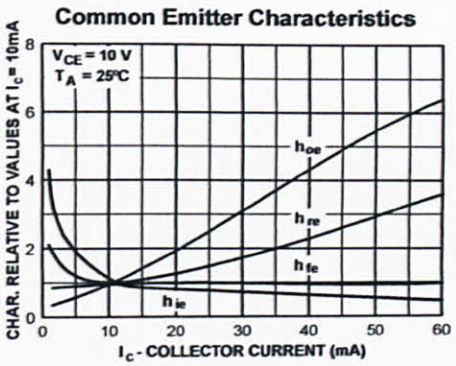



Figure 4. Common Emitter Characteristics

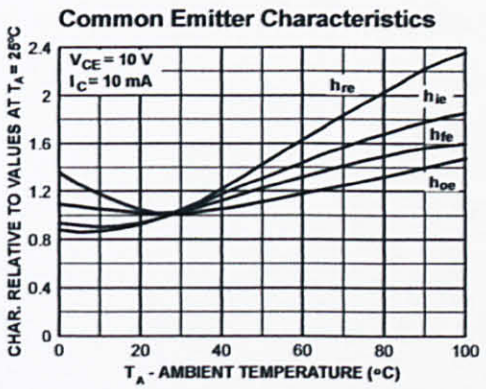



Figure 5. Common Emitter Characteristics

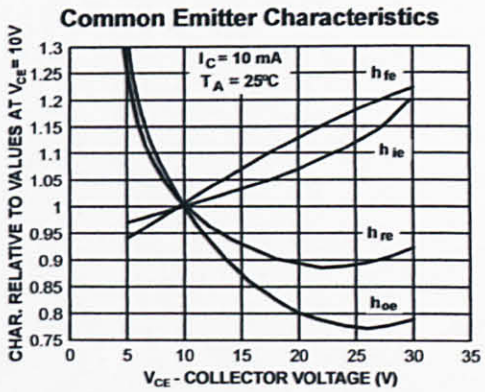



Figure 6. Common Emitter Characteristics

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Fairchild Semiconductor®
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FACT®
FAST®
FastvCore™
FPS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
*i-Lo™*
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power220®
Power247®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®
UniFET™
VCX™

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |

Rev. I31

# APPENDIX C

# TL494 PULSE-WIDTH-MODULATION CONTROL CIRCUITS DATA SHEET

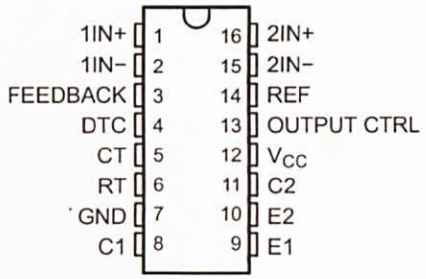
# TL494
# PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS074E–JANUARY 1983–REVISED FEBRUARY 2005

## FEATURES

- **Complete PWM Power-Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance**
- **Circuit Architecture Allows Easy Synchronization**

**D, DB, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

The TL494 incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application.

The TL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from –0.3 V to $V_{CC}$ – 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 provides for push-pull or single-ended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494C is characterized for operation from 0°C to 70°C. The TL494I is characterized for operation from –40°C to 85°C.

### AVAILABLE OPTIONS

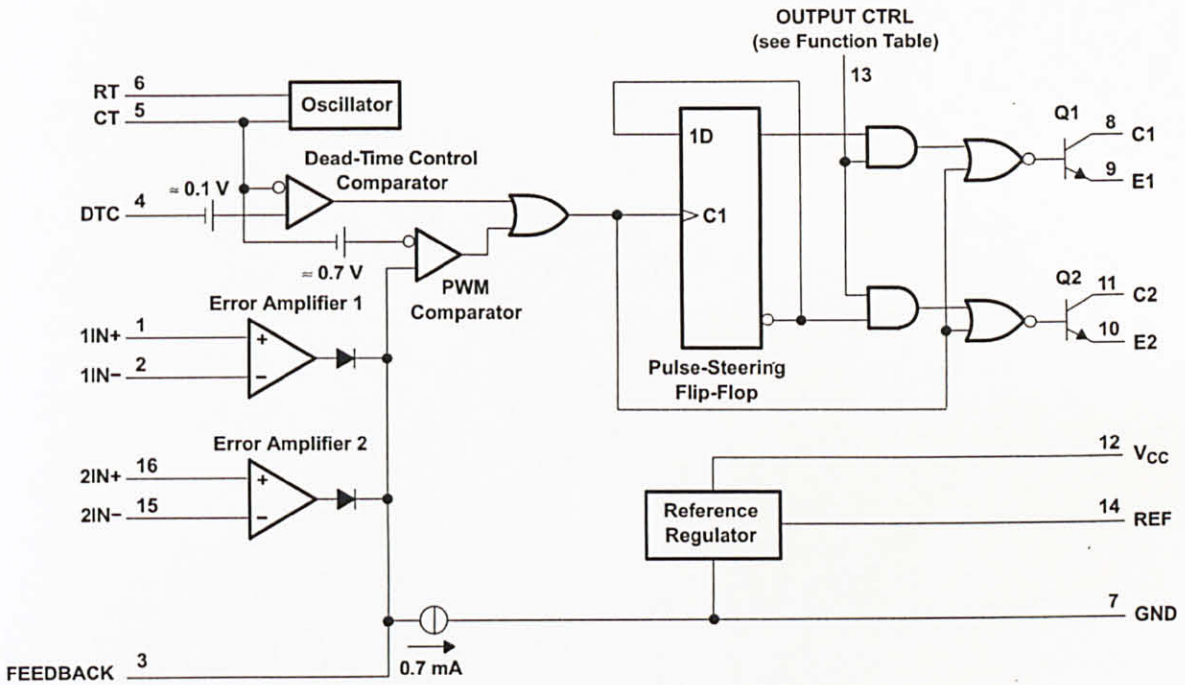
| $T_A$ | PACKAGED DEVICES(1) | | | | |
|---|---|---|---|---|---|
| | SMALL OUTLINE (D) | PLASTIC DIP (N) | SMALL OUTLINE (NS) | SHRINK SMALL OUTLINE (DB) | THIN SHRINK SMALL OUTLINE (PW) |
| 0°C to 70°C | TL494CD | TL494CN | TL494CNS | TL494CDB | TL494CPW |
| –40°C to 85°C | TL494ID | TL494IN | — | — | — |

(1) The D, DB, NS, and PW packages are available taped and reeled. Add the suffix R to device type (e.g., TL494CDR).

## FUNCTION TABLE

| INPUT TO OUTPUT CTRL | OUTPUT FUNCTION |
|---|---|
| $V_I$ = GND | Single-ended or parallel output |
| $V_I$ = $V_{ref}$ | Normal push-pull operation |

## FUNCTIONAL BLOCK DIAGRAM



## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage(2) | | | 41 | V |
| $V_I$ | Amplifier input voltage | | | $V_{CC}$ + 0.3 | V |
| $V_O$ | Collector output voltage | | | 41 | V |
| $I_O$ | Collector output current | | | 250 | mA |
| $\theta_{JA}$ | Package thermal impedance(3)(4) | D package | | 73 | °C/W |
| | | DB package | | 82 | |
| | | N package | | 67 | |
| | | NS package | | 64 | |
| | | PW package | | 108 | |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | | 260 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the network ground terminal.
(3) Maximum power disipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperatire is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 7 | 40 | V |
| $V_I$ | Amplifier input voltage | | –0.3 | $V_{CC}$ – 2 | V |
| $V_O$ | Collector output voltage | | | 40 | V |
| | Collector output current (each transistor) | | | 200 | mA |
| | Current into feedback terminal | | | 0.3 | mA |
| $f_{OSC}$ | Oscillator frequency | | 1 | 300 | kHz |
| $C_T$ | Timing capacitor | | 0.47 | 10000 | nF |
| $R_T$ | Timing resistor | | 1.8 | 500 | kΩ |
| $T_A$ | Operating free-air temperature | TL494C | 0 | 70 | °C |
| | | TL494I | –40 | 85 | |

## Electrical Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 15 V, f = 10 kHz (unless otherwise noted)

### Reference Section

| PARAMETER | TEST CONDITIONS(1) | TL494C, TL494I | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP(2) | MAX | |
| Output voltage (REF) | $I_O$ = 1 mA | 4.75 | 5 | 5.25 | V |
| Input regulation | $V_{CC}$ = 7 V to 40 V | | 2 | 25 | mV |
| Output regulation | $I_O$ = 1 mA to 10 mA | | 1 | 15 | mV |
| Output voltage change with temperature | $\Delta T_A$ = MIN to MAX | | 2 | 10 | mV/V |
| Short-circuit output current(3) | REF = 0 V | | 25 | | mA |

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values, except for parameter changes with temperature, are at $T_A$ = 25°C.
(3) Duration of short circuit should not exceed one second.

### Oscillator Section

$C_T$ = 0.01 µF, $R_T$ = 12 kΩ (see Figure 1)

| PARAMETER | TEST CONDITIONS(1) | TL494C, TL494I | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP(2) | MAX | |
| Frequency | | | 10 | | kHz |
| Standard deviation of frequency(3) | All values of $V_{CC}$, $C_T$, $R_T$, and $T_A$ constant | | 100 | | Hz/kHz |
| Frequency change with voltage | $V_{CC}$ = 7 V to 40 V, $T_A$ = 25°C | | 1 | | Hz/kHz |
| Frequency change with temperature(4) | $\Delta T_A$ = MIN to MAX | | | 10 | Hz/kHz |

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values, except for parameter changes with temperature, are at $T_A$ = 25°C.
(3) Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

(4) Temperature coefficient of timing capacitor and timing resistor are not taken into account.

### Error-Amplifier Section

See Figure 2

| PARAMETER | TEST CONDITIONS | TL494C, TL494I | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP(1) | MAX | |
| Input offset voltage | $V_O$ (FEEDBACK) = 2.5 V | | 2 | 10 | mV |
| Input offset current | $V_O$ (FEEDBACK) = 2.5 V | | 25 | 250 | nA |
| Input bias current | $V_O$ (FEEDBACK) = 2.5 V | | 0.2 | 1 | µA |
| Common-mode input voltage range | $V_{CC}$ = 7 V to 40 V | –0.3 to $V_{CC}$ – 2 | | | V |
| Open-loop voltage amplification | $\Delta V_O$ = 3 V, $V_O$ = 0.5 V to 3.5 V, $R_L$ = 2 kΩ | 70 | 95 | | dB |
| Unity-gain bandwidth | $V_O$ = 0.5 V to 3.5 V, $R_L$ = 2 kΩ | | 800 | | kHz |
| Common-mode rejection ratio | $\Delta V_O$ = 40 V, $T_A$ = 25°C | 65 | 80 | | dB |
| Output sink current (FEEDBACK) | $V_{ID}$ = –15 mV to –5 V, V (FEEDBACK) = 0.7 V | 0.3 | 0.7 | | mA |
| Output source current (FEEDBACK) | $V_{ID}$ = 15 mV to 5 V, V (FEEDBACK) = 3.5 V | –2 | | | mA |

(1) All typical values, except for parameter changes with temperature, are at $T_A$ = 25°C.

## Electrical Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 15 V, f = 10 kHz (unless otherwise noted)

### Output Section

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| Collector off-state current | | $V_{CE}$ = 40 V, $V_{CC}$ = 40 V | | 2 | 100 | μA |
| Emitter off-state current | | $V_{CC}$ = $V_C$ = 40 V, $V_E$ = 0 | | | –100 | μA |
| Collector-emitter saturation voltage | Common emitter | $V_E$ = 0, $I_C$ = 200 mA | | 1.1 | 1.3 | V |
| | Emitter follower | $V_{O(C1 \text{ or } C2)}$ = 15 V, $I_E$ = –200 mA | | 1.5 | 2.5 | |
| Output control input current | | $V_I$ = $V_{ref}$ | | | 3.5 | mA |

(1) All typical values, except for temperature coefficient, are at $T_A$ = 25°C.

### Dead-Time Control Section

See Figure 1

| PARAMETER | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|
| Input bias current (DEAD-TIME CTRL) | $V_I$ = 0 to 5.25 V | | –2 | –10 | μA |
| Maximum duty cycle, each output | $V_I$ (DEAD-TIME CTRL) = 0, $C_T$ = 0.01 μF, $R_T$ = 12 kΩ | | 45 | | % |
| Input threshold voltage (DEAD-TIME CTRL) | Zero duty cycle | | 3 | 3.3 | V |
| | Maximum duty cycle | 0 | | | |

(1) All typical values, except for temperature coefficient, are at $T_A$ = 25°C.

### PWM Comparator Section

See Figure 1

| PARAMETER | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|
| Input threshold voltage (FEEDBACK) | Zero duty cyle | | 4 | 4.5 | V |
| Input sink current (FEEDBACK) | V (FEEDBACK) = 0.7 V | 0.3 | 0.7 | | mA |

(1) All typical values, except for temperature coefficient, are at $T_A$ = 25°C.

### Total Device

| PARAMETER | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| Standby supply current | $R_T$ = $V_{ref}$, All other inputs and outputs open | $V_{CC}$ = 15 V | | 6 | 10 | mA |
| | | $V_{CC}$ = 40 V | | 9 | 15 | |
| Average supply current | $V_I$ (DEAD-TIME CTRL) = 2 V, See Figure 1 | | | 7.5 | | mA |

(1) All typical values, except for temperature coefficient, are at $T_A$ = 25°C.

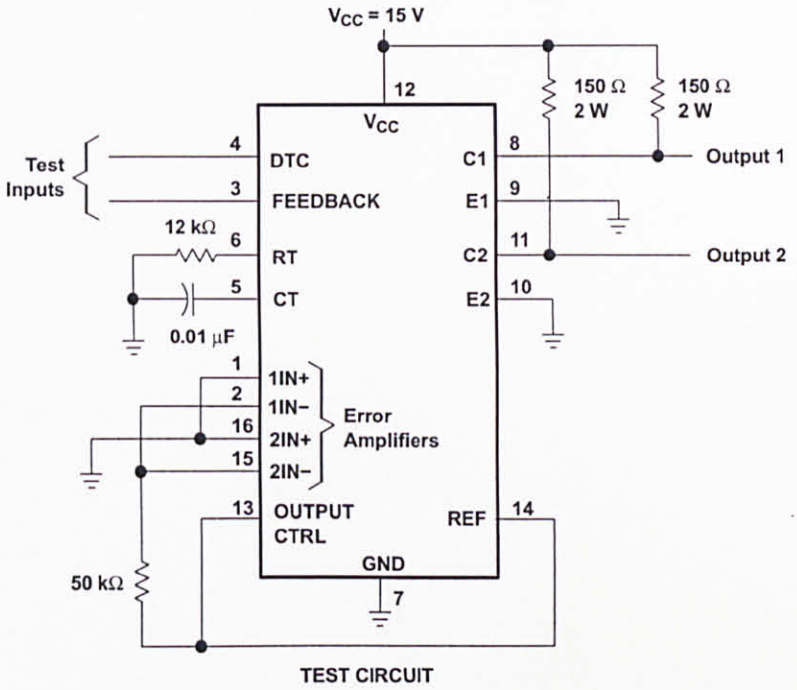
### Switching Characteristics

$T_A$ = 25°C

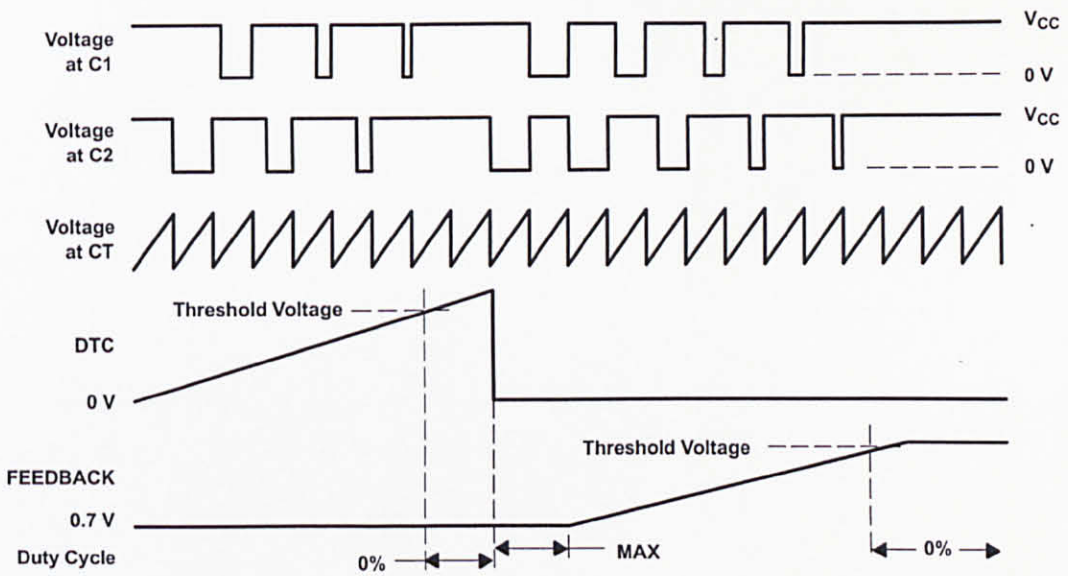
| PARAMETER | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|
| Rise time | Common-emitter configuration, See Figure 3 | | 100 | 200 | ns |
| Fall time | | | 25 | 100 | ns |
| Rise time | Emitter-follower configuration, See Figure 4 | | 100 | 200 | ns |
| Fall time | | | 40 | 100 | ns |

(1) All typical values, except for temperature coefficient, are at $T_A$ = 25°C.

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

**Figure 1. Operational Test Circuit and Waveforms**

## PARAMETER MEASUREMENT INFORMATION

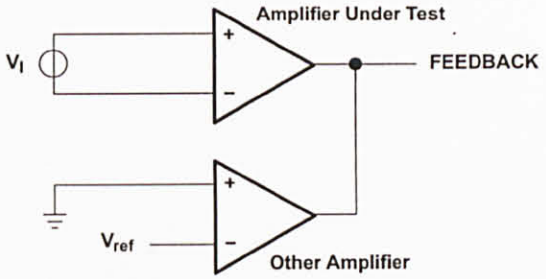
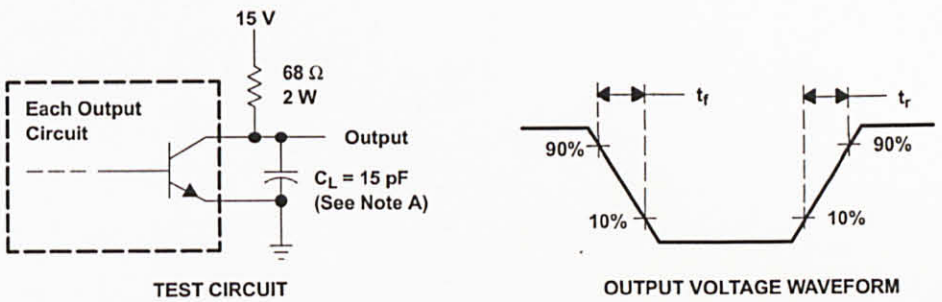
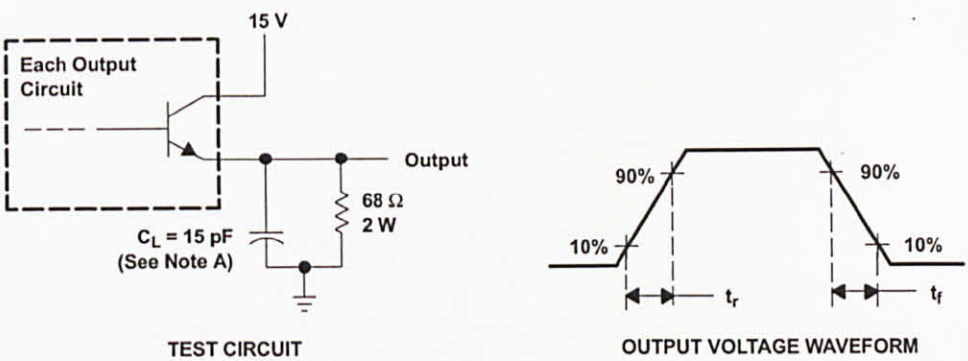



**Figure 2. Amplifier Characteristics**




NOTE A: $C_L$ includes probe and jig capacitance.

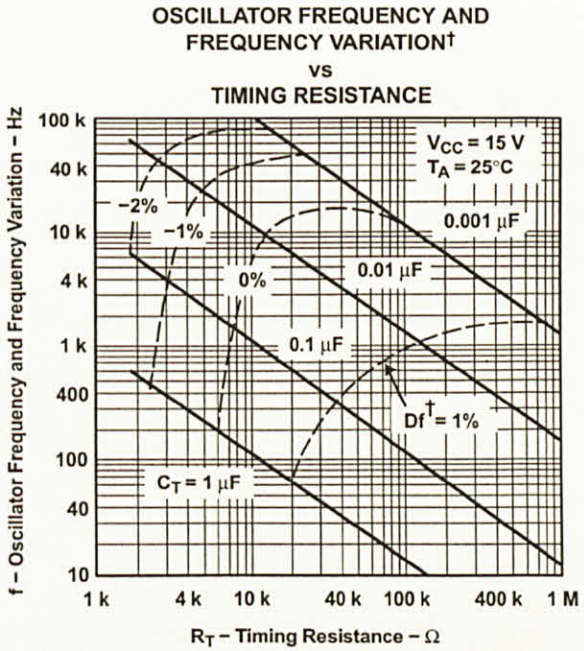
**Figure 3. Common-Emitter Configuration**




NOTE A: $C_L$ includes probe and jig capacitance.

**Figure 4. Emitter-Follower Configuration**

## TYPICAL CHARACTERISTICS




† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

**Figure 5.**

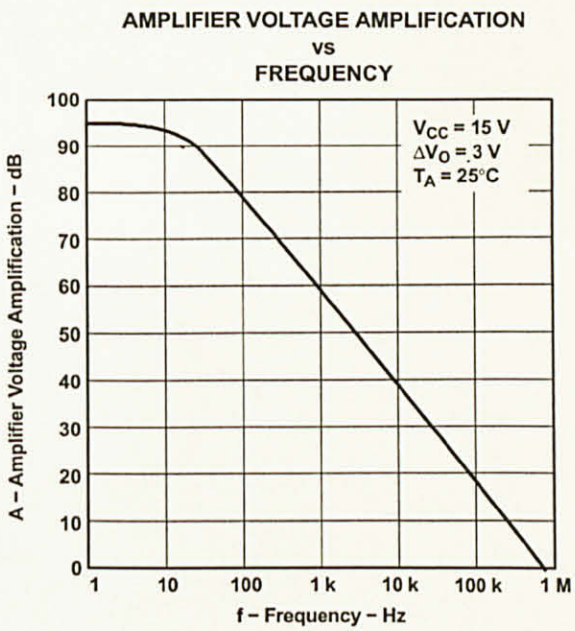



**Figure 6.**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| TL494CD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CDBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CDBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CDBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CDE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| TL494CN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL494CNE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL494CNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CPWLE | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI |
| TL494CPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494CPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494ID | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494IDE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494IDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494IDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494IDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| | | | | | | no Sb/Br) | | |
| TL494IDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL494IN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL494INE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL494MJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| TL494MJB | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |

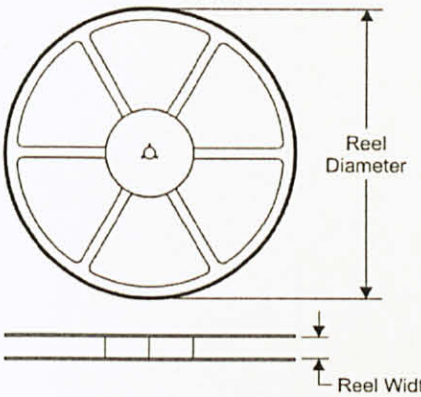
[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

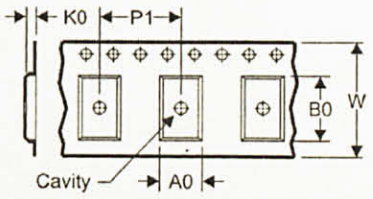
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

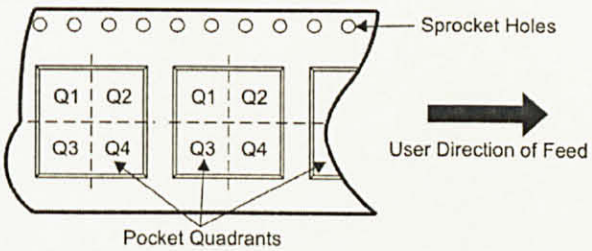



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

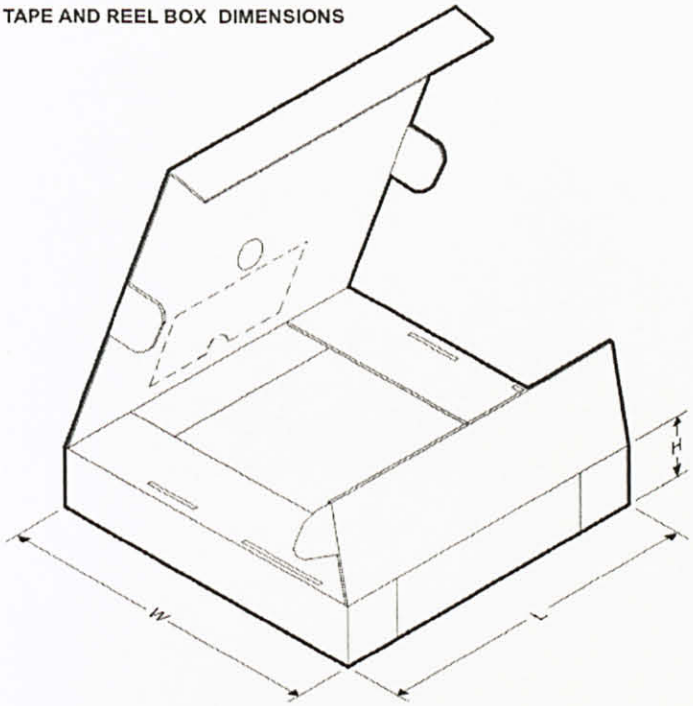
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL494CDBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| TL494CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TL494CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TL494CNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TL494CPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL494IDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



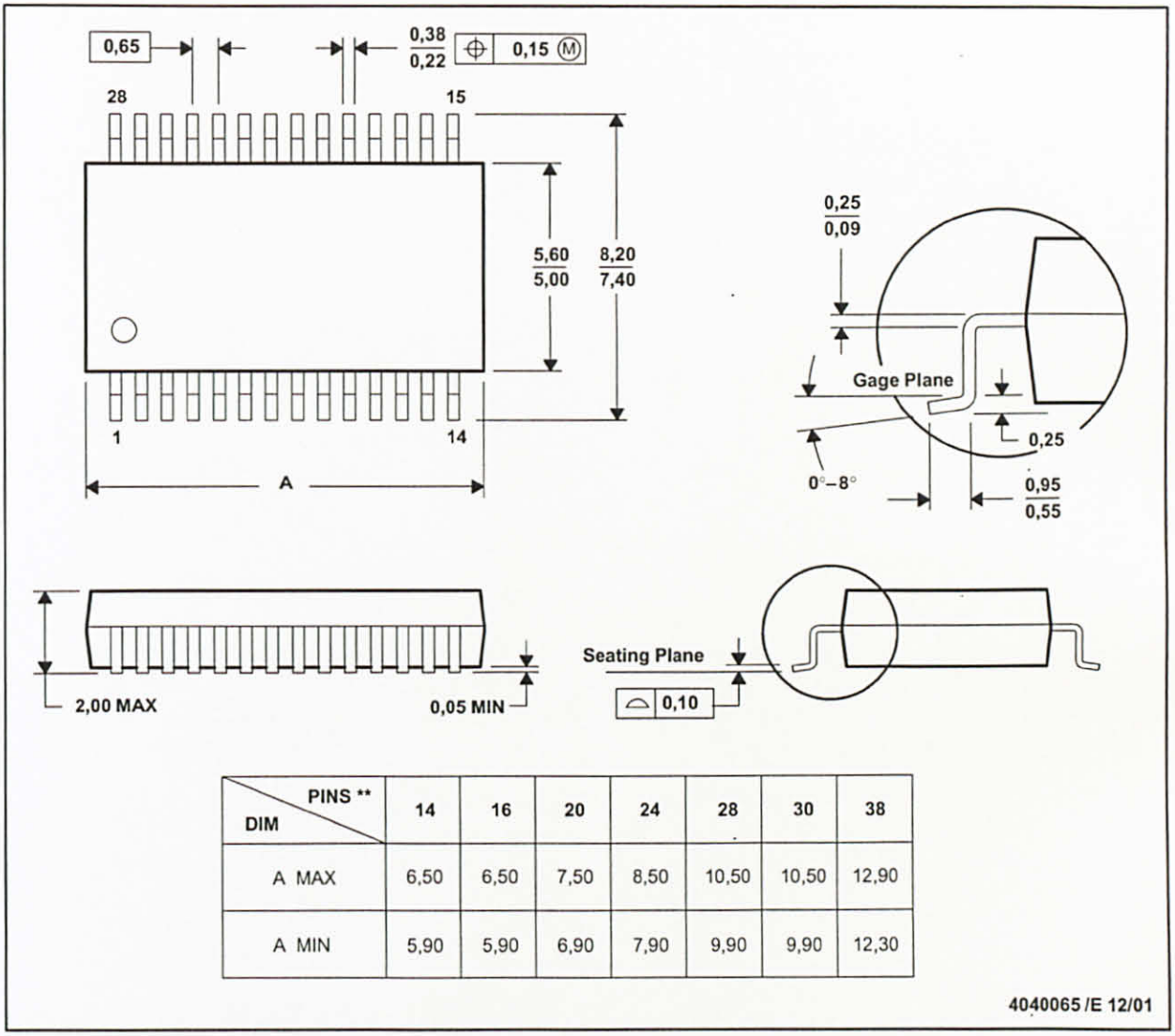

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL494CDBR | SSOP | DB | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| TL494CDR | SOIC | D | 16 | 2500 | 346.0 | 346.0 | 33.0 |
| TL494CDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| TL494CNSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| TL494CPWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |
| TL494IDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

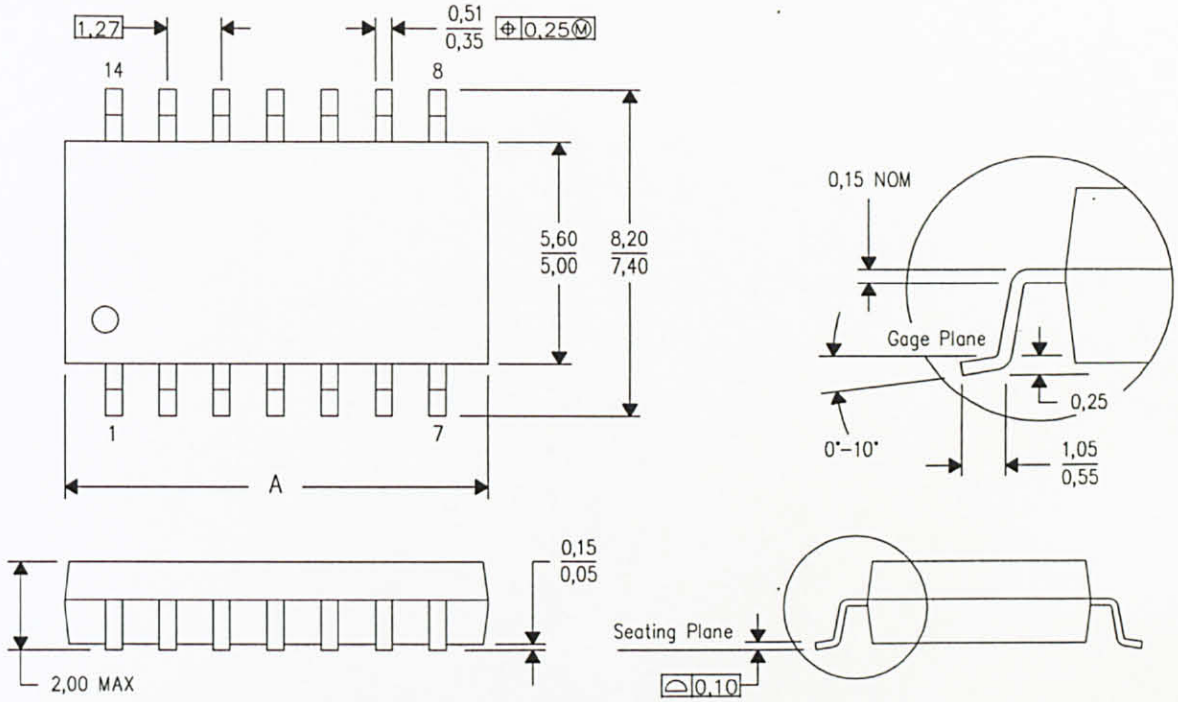
**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

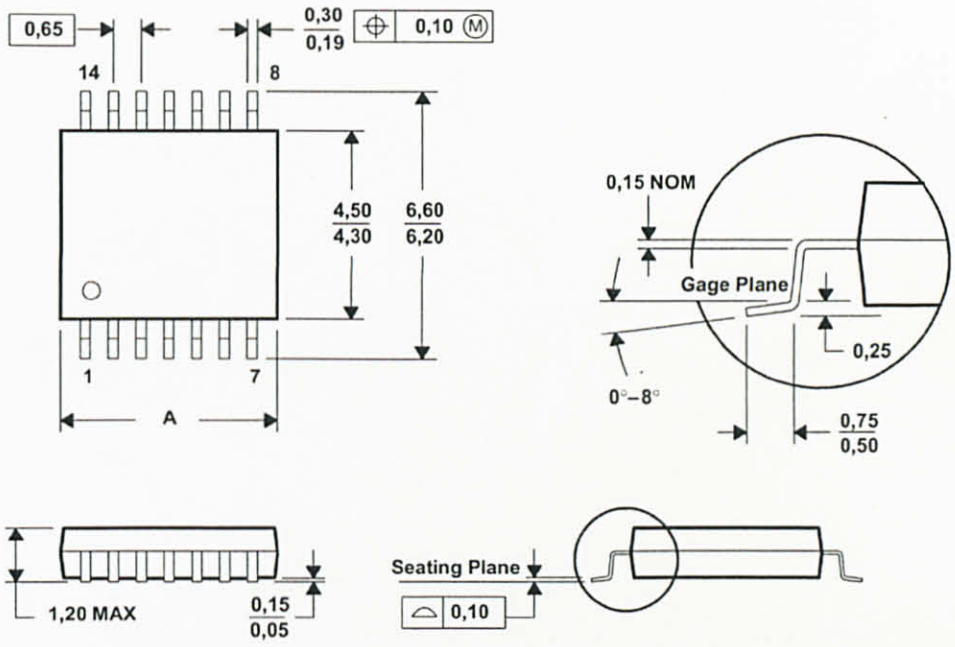
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

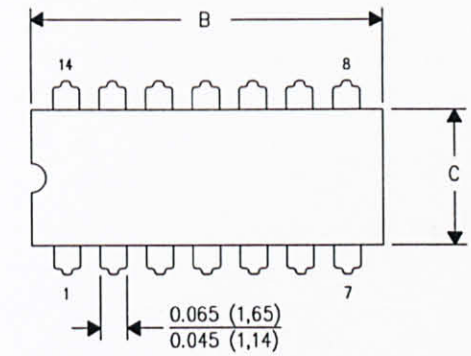
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

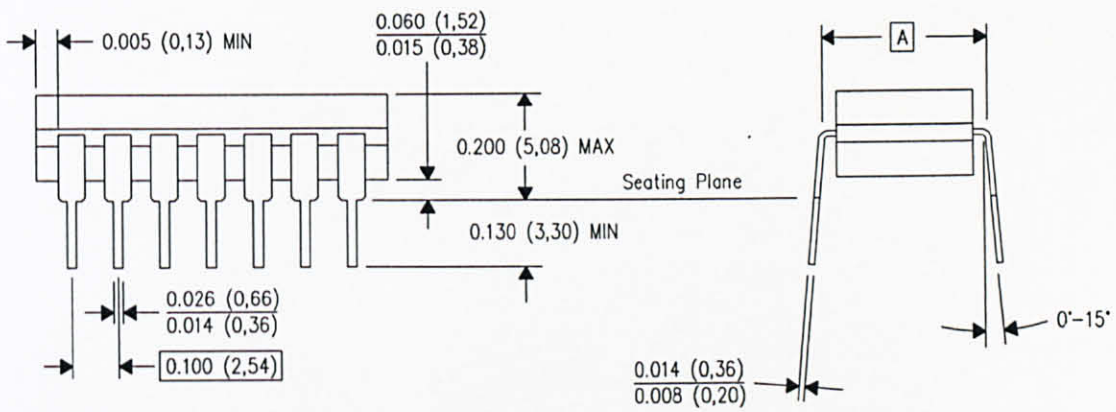
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

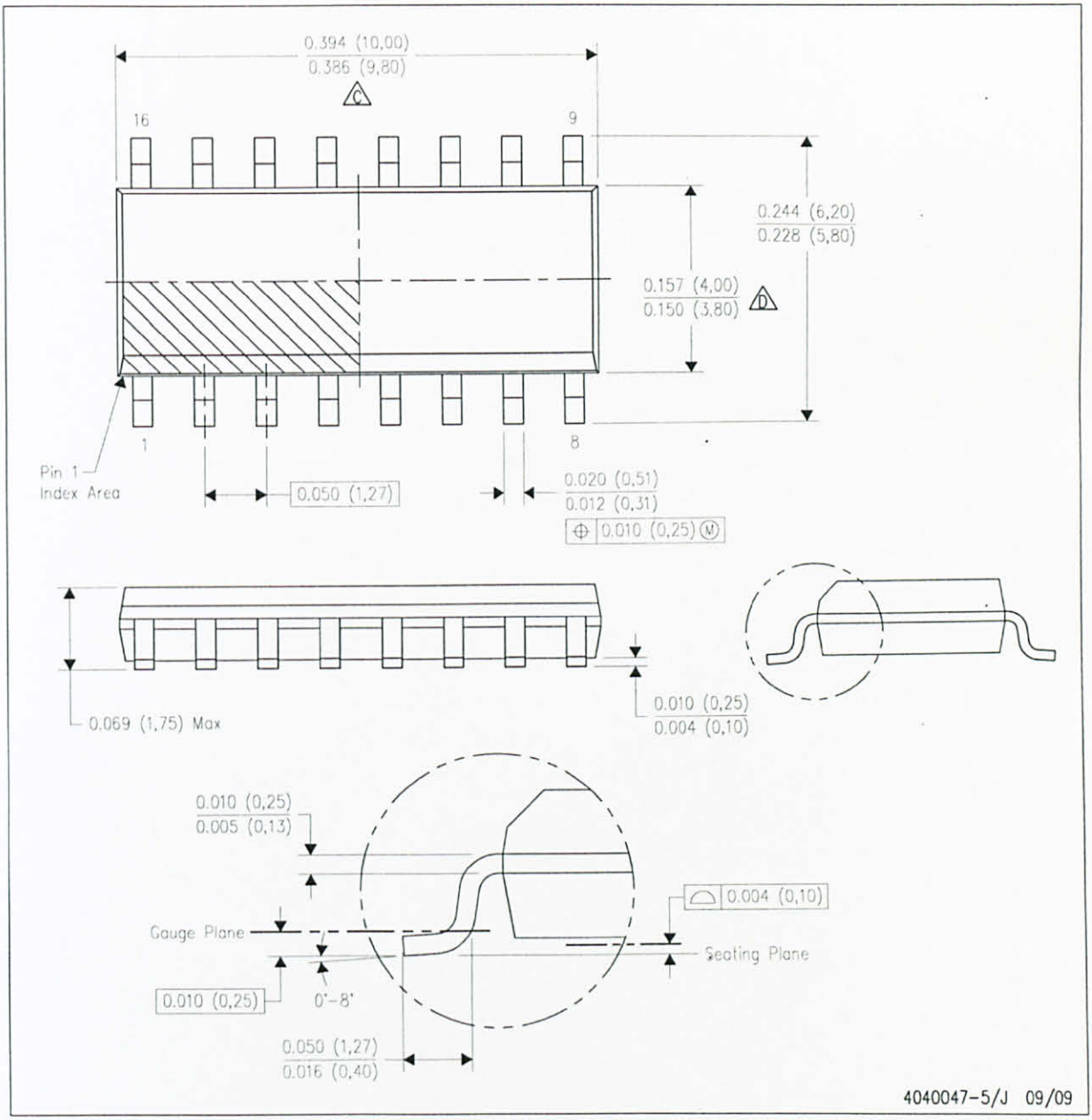



4040083/F 03/03

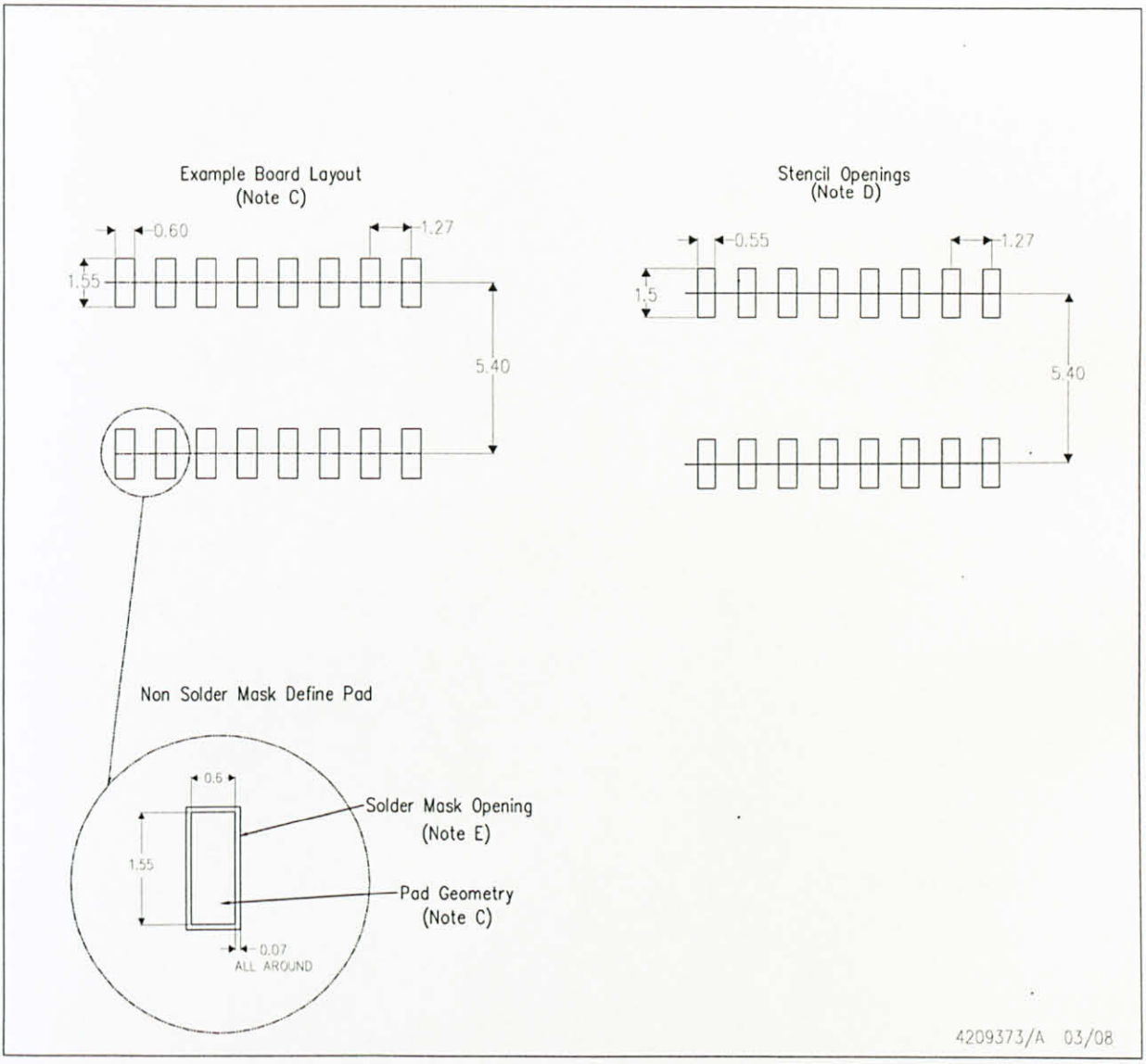
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

D (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AC.

D(R–PDSO–G16)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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# APPENDIX D

# UC3823A HIGH-SPEED PWM CONTROLLER DATA SHEET



# HIGH-SPEED PWM CONTROLLER

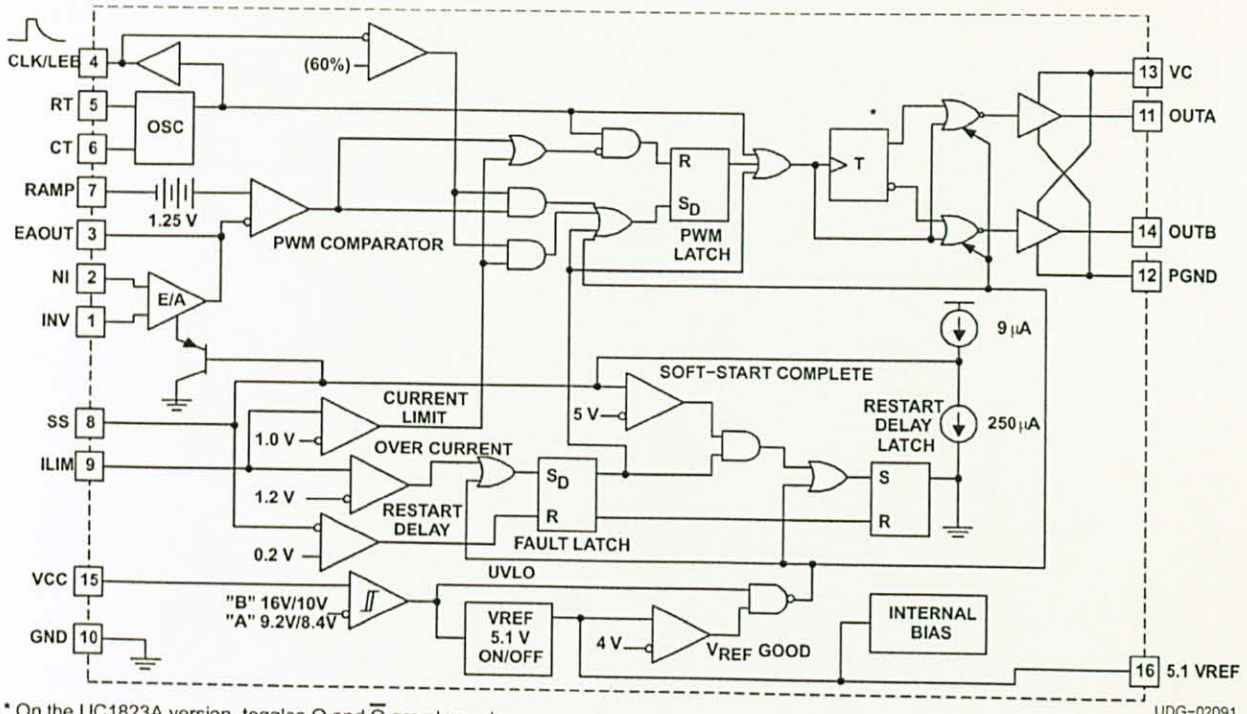
## FEATURES

- Improved Versions of the UC3823/UC3825 PWMs
- Compatible with Voltage-Mode or Current-Mode Control Methods
- Practical Operation at Switching Frequencies to 1 MHz
- 50-ns Propagation Delay to Output
- High-Current Dual Totem Pole Outputs (2-A Peak)
- Trimmed Oscillator Discharge Current
- Low 100-μA Startup Current
- Pulse-by-Pulse Current Limiting Comparator
- Latched Overcurrent Comparator With Full Cycle Restart

## DESCRIPTION

The UC3823A and UC3823B and the UC3825A and UC3825B family of PWM controllers are improved versions of the standard UC3823 and UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset voltage is 2 mV. Current limit threshold is assured to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100 μA, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2-A peak currents during transitions.

## BLOCK DIAGRAM




* On the UC1823A version, toggles Q and $\overline{Q}$ are always low.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2 V. The overcurrent comparator sets a latch that ensures full discharge of the soft-start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft-start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 CLOCK pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC3825A and UC3825B have dual alternating outputs and the same pin configuration of the UC3825. The UC3823A and UC3823B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the UC3823A and UC3823B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. "A" version parts have UVLO thresholds identical to the original UC3823 and UC3825. The "B" versions have UVLO thresholds of 16 V and 10 V, intended for ease of use in off-line applications.

Consult the application note, *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers*, (SLUA125) for detailed technical and applications information.

## ORDERING INFORMATION

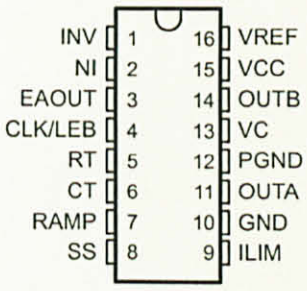
| $T_A$ | MAXIMUM DUTY CYCLE | UVLO | | | | | |
|---|---|---|---|---|---|---|---|
| | | 9.2 V / 8.4 V | | | 16 V / 10 V | | |
| | | SOIC-16(1) (DW) | PDIP-16 (N) | PLCC-20(1) (Q) | SOIC-16 (DW) | PDIP-16 (N) | PLCC-20(1) (Q) |
| −40°C to 85°C | < 100% | UC2823ADW | UC2823AN | UC2823AQ | UC2823BDW | UC2823BN | – |
| | < 50% | UC2825ADW | UC2825AN | UC2825AQ | UC2825BDW | UC2825BN | – |
| −0°C to 70°C | < 100% | UC3823ADW | UC3823AN | UC3823AQ | UC3823BDW | UC3823BN | – |
| | < 50% | UC3825ADW | UC3825AN | UC3825AQ | UC3825BDW | UC3825BN | UC3825BQ |

(1) The DW and Q packages are also available taped and reeled. Add TR suffix to the device type (i.e., UC2823ADWR). To order quantities of 1000 devices per reel for the Q package and 2000 devices per reel for the DW package.

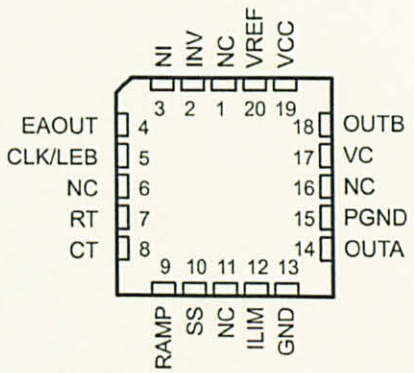
| $T_A$ | MAXIMUM DUTY CYCLE | UVLO | |
|---|---|---|---|
| | | 9.2 V / 8.4 V | |
| | | CDIP-16 (J) | LCCC-20 (L) |
| −55°C to 125°C | < 100% | UC1823AJ, UC1823AJ883B, UC1823AJQMLV | UC1823AL, UC1823AL883B |
| | < 50% | UC1825AJ, UC1825AJ883B, UC1825AJQMLV | UC1825AL, UC1825AL883B, UC1825ALQMLV |

## PIN ASSIGNMENTS

DW, J, OR N PACKAGES
(TOP VIEW)




Q OR L PACKAGES
(TOP VIEW)




NC = no connection

## TERMINAL FUNCTIONS

| TERMINAL | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| | J or DW | Q or L | | |
| CLK/LEB | 4 | 5 | O | Output of the internal oscillator |
| CT | 6 | 8 | I | Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length. |
| EAOUT | 3 | 4 | O | Output of the error amplifier for compensation |
| GND | 10 | 13 | – | Analog ground return pin |
| ILIM | 9 | 12 | I | Input to the current limit comparator |
| INV | 1 | 2 | I | Inverting input to the error amplifier |
| NI | 2 | 3 | I | Non-inverting input to the error amplifier |
| OUTA | 11 | 14 | O | High current totem pole output A of the on-chip drive stage. |
| OUTB | 14 | 18 | O | High current totem pole output B of the on-chip drive stage. |
| PGND | 12 | 15 | – | Ground return pin for the output driver stage |
| RAMP | 7 | 9 | I | Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input. |
| RT | 5 | 7 | I | Timing resistor connection pin for oscillator frequency programming |
| SS | 8 | 10 | I | Soft-start input pin which also doubles as the maximum duty cycle clamp. |
| VC | 13 | 17 | – | Power supply pin for the output stage. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths. |
| VCC | 15 | 19 | – | Power supply pin for the device. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths |
| VREF | 16 | 20 | O | 5.1-V reference. For stability, the reference should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane. |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | | UNIT |
|---|---|---|---|
| $V_{IN}$ | Supply voltage, | VC, VCC | 22 V |
| $I_O$ | Source or sink current, DC | OUTA, OUTB | 0.5 A |
| $I_O$ | Source or sink current, pulse (0.5 μs) | OUTA, OUTB | 2.2 A |
| | Analog inputs | INV, NI, RAMP | −0.3 V to 7 V |
| | | ILIM, SS | −0.3 V to 6 V |
| | Power ground | PGND | ±0.2 V |
| | Outputs | OUTA, OUTB limits | PGND −0.3 V to $V_C$ +0.3 V |
| $I_{CLK}$ | Clock output current | CLK/LEB | −5 mA |
| $I_{O(EA)}$ | Error amplifier output current | EAOUT | 5 mA |
| $I_{SS}$ | Soft-start sink current | SS | 20 mA |
| $I_{OSC}$ | Oscillator charging current | RT | −5 mA |
| $T_J$ | Operating virtual junction temperature range | | −55°C to 150°C |
| $T_{stg}$ | Storage temperature | | −65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | −55C°C to 150°C |
| $t_{STG}$ | Storage temperature | | −65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds | | 300°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$T_A$ = −55°C to 125°C for the UC1823A/UC1825A, $T_A$ = −40°C to 85°C for the UC2823x/UC2825x, $T_A$ = 0°C to 70°C for the UC3823x/UC3825x, $R_T$ = 3.65 kΩ, $C_T$ = 1 nF, $V_{CC}$ = 12 V, $T_A$ = $T_J$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **REFERENCE, $V_{REF}$** | | | | | | |
| $V_O$ | Ouput voltage range | $T_J$ = 25°C, $I_O$ = 1 mA | 5.05 | 5.1 | 5.15 | V |
| | Line regulation | 12 V ≤ VCC ≤ 20 V | | 2 | 15 | mV |
| | Load regulation | 1 mA ≤ $I_O$ ≤ 10 mA | | 5 | 20 | |
| | Total output variation | Line, load, temperature | 5.03 | | 5.17 | V |
| | Temperature stability(1) | $T_{(min)}$ < $T_A$ < $T_{(max)}$ | | 0.2 | 0.4 | mV/°C |
| | Output noise voltage(1) | 10 Hz < f < 10 kHz | | 50 | | $\mu V_{RMS}$ |
| | Long term stability(1) | $T_J$ = 125°C, 1000 hours | | 5 | 25 | mV |
| | Short circuit current | VREF = 0 V | 30 | 60 | 90 | mA |
| **OSCILLATOR** | | | | | | |
| $f_{OSC}$ | Initial accuracy(1) | $T_J$ = 25°C | 375 | 400 | 425 | kHz |
| | | $R_T$ = 6.6 kΩ, $C_T$ = 220 pF, $T_A$ = 25°C | 0.9 | 1 | 1.1 | MHz |
| | Total variation(1) | Line, temperature | 350 | | 450 | kHz |
| | | $R_T$ = 6.6 kΩ, $C_T$ = 220 pF, | 0.85 | | 1.15 | MHz |
| | Voltage stability | 12 V < VCC < 20 V | | | 1% | |
| | Temperature stability(1) | $T_{(min)}$ < $T_A$ < $T_{(max)}$ | +/− | 5% | | |
| | High-level output voltage, clock | | 3.7 | 4 | | V |
| | Low-level output voltage, clock | | | 0 | 0.2 | |
| | Ramp peak | | 2.6 | 2.8 | 3 | |
| | Ramp valley | | 0.7 | 1 | 1.25 | |
| | Ramp valley-to-peak | | 1.6 | 1.8 | 2 | |
| $I_{OSC}$ | Oscillator discharge current | $R_T$ = OPEN, $V_{CT}$ = 2 V | 9 | 10 | 11 | mA |
| **ERROR AMPLIFIER** | | | | | | |
| | Input offset voltage | | | 2 | 10 | mV |
| | Input bias current | | | 0.6 | 3 | µA |
| | Input offset current | | | 0.1 | 1 | |
| | Open loop gain | 1 V < $V_O$ < 4 V | 60 | 95 | | dB |
| CMRR | Common mode rejection ratio | 1.5 V < $V_{CM}$ < 5.5 V | 75 | 95 | | |
| PSRR | Power supply rejection ratio | 12 V < $V_{CC}$ < 20 V | 85 | 110 | | |
| $I_{O(sink)}$ | Output sink current | $V_{EAOUT}$ = 1 V | 1 | 2.5 | | mA |
| $I_{O(src)}$ | Output source current | $V_{EAOUT}$ = 4 V | −0.5 | −1.3 | | |
| | High-level output voltage | $I_{EAOUT}$ = −0.5 mA | 4.5 | 4.7 | 5 | V |
| | Low-level output voltage | $I_{EAOUT}$ = −1 mA | 0 | 0.5 | 1 | |
| | Gain bandwidth product | f = 200 kHz | 6 | 12 | | Mhz |
| | Slew rate(1) | | 6 | 9 | | V/µs |

(1) Ensured by design. Not production tested.

## ELECTRICAL CHARACTERISTICS

$T_A$ = −55°C to 125°C for the UC1823A/UC1825A, $T_A$ = −40°C to 85°C for the UC2823x/UC2825x, $T_A$ = 0°C to 70°C for the UC3823x/UC3825x, $R_T$ = 3.65 kΩ, $C_T$ = 1 nF, $V_{CC}$ = 12 V, $T_A$ = $T_J$ (unless otherwise noted)

| | | | | | | |
|---|---|---|---|---|---|---|
| **PWM COMPARATOR** | | | | | | |
| $I_{BIAS}$ | Bias current, RAMP | $V_{RAMP}$ = 0 V | | −1 | −8 | µA |
| | Minimum duty cycle | | | | 0% | |
| | Maximum duty cycle | | 85% | | | |
| $t_{LEB}$ | Leading edge blanking time | $R_{LEB}$ = 2 kΩ, $C_{LEB}$ = 470 pF | 300 | 375 | 450 | ns |
| $R_{LEB}$ | Leading edge blanking resistance | $V_{CLK/LEB}$ = 3 V | 8.5 | 10.0 | 11.5 | kΩ |
| $V_{ZDC}$ | Zero dc threshold voltage, EAOUT | $V_{RAMP}$ = 0 V | 1.10 | 1.25 | 1.4 | V |
| $t_{DELAY}$ | Delay-to-output time | $V_{EAOUT}$ = 2.1 V, $V_{ILIM}$ = 0 V to 2 V step | | 50 | 80 | ns |
| **CURRENT LIMIT / START SEQUENCE / FAULT** | | | | | | |
| $I_{SS}$ | Soft-start charge current | $V_{SS}$= 2.5 V | 8 | 14 | 20 | µA |
| $V_{SS}$ | Full soft-start threshold voltage | | 4.3 | 5 | | V |
| $I_{DSCH}$ | Restart discharge current | $V_{SS}$= 2.5 V | 100 | 250 | 350 | µA |
| $I_{SS}$ | Restart threshold voltage | | | 0.3 | 0.5 | V |
| $I_{BIAS}$ | ILIM bias current | $V_{ILIM}$ = 0 V to 2 V step | | | 15 | µA |
| $I_{CL}$ | Current limit threshold voltage | | 0.95 | 1 | 1.05 | V |
| | Overcurrent threshold voltage | | 1.14 | 1.2 | 1.26 | |
| $t_d$ | Delay-to-output time, ILIM(1) | $V_{ILIM}$ = 0 V to 2 V step | | 50 | 80 | ns |
| **OUTPUT** | | | | | | |
| | Low-level output saturation voltage | $I_{OUT}$ = 20 mA | | 0.25 | 0.4 | V |
| | | $I_{OUT}$ = 200 mA | | 1.2 | 2.2 | |
| | High-level output saturation voltage | $I_{OUT}$ = 20 mA | | 1.9 | 2.9 | |
| | | $I_{OUT}$ = 200 mA | | 2 | 3 | |
| $t_r$, $t_f$ | Rise/fall time(1) | $C_L$ = 1 nF | | 20 | 45 | ns |
| **UNDERVOLTAGE LOCKOUT (UVLO)** | | | | | | |
| | Start threshold voltage | UC2823B, UC2825B, UC3825B, UC3825B | | 16 | 17 | V |
| | | UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A | 8.4 | 9.2 | 9.6 | |
| | Stop threshold voltage | UC2823B, UC2825B, UC3825B, UC3825B | 9 | 10 | | |
| | OVLO hysteresis | UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A | 0.4 | 0.8 | 1.2 | |
| | | UC2823B, UC2825B, UC3825B, UC3825B | 5 | 6 | 7 | |
| **SUPPLY CURRENT** | | | | | | |
| $I_{su}$ | Startup current | VC = VCC = $V_{TH}$ = −0.5 V | | 100 | 300 | µA |
| $I_{CC}$ | Input current | | | 28 | 36 | mA |

(1) Ensured by design. Not production tested.

## APPLICATION INFORMATION

The oscillator of the UC3823A, UC3823B, UC3825A, and UC3825B is a saw tooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin ($C_{CT}$). The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency (RT) and $D_{MAX}$. The design equations are:

$$R_T = \frac{3\ V}{(10\ mA) \times (1 - D_{MAX})} \qquad C_T = \frac{(1.6 \times D_{MAX})}{(R_T \times f)} \tag{1}$$

Recommended values for $R_T$ range from 1 kΩ to 100 kΩ. Control of $D_{MAX}$ less than 70% is not recommended.

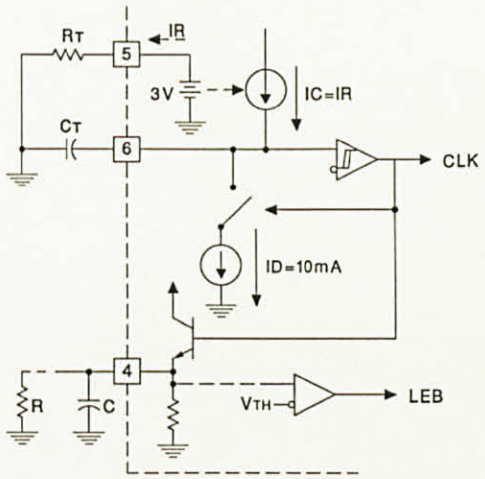



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**Figure 1. Oscillator**

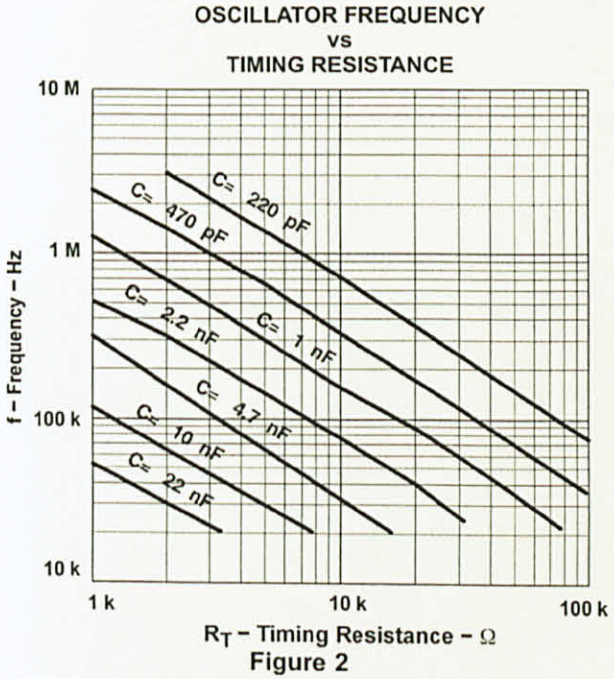


**Figure 2**

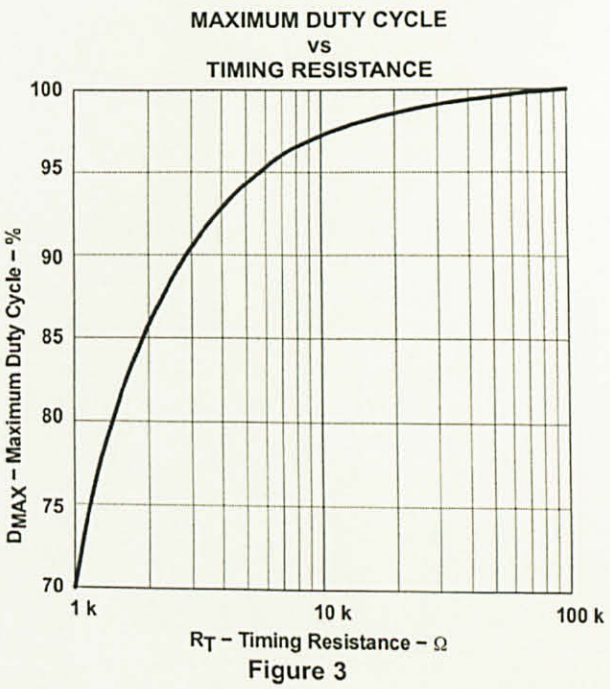


**Figure 3**

## LEADING EDGE BLANKING

The UC3823A, UC2823B, UC3825A, and UC3825B perform fixed frequency pulse width modulation control. The UC3823A, and UC3823B outputs operate together at the switching frequency and can vary from zero to some value less than 100%. The UC3825A and UC3825B outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a leading edge blanking (LEB) period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-kΩ resistor determines the blanked interval. The 10-kΩ resistor has a 10% tolerance. For more accuracy, an external 2-kΩ 1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 kΩ with a tolerance of 2.4%. The design equation is:

$$t_{LEB} = 0.5 \times (R \parallel 10\ k\Omega) \times C \qquad (2)$$

Values of R less than 2 kΩ should not be used.

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.

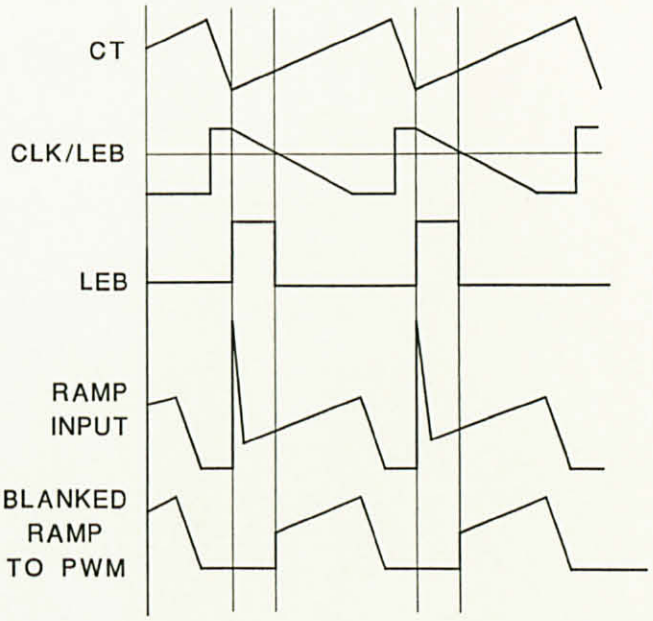


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**Figure 4. Leading Edge Blanking Operational Waveforms**

## UVLO, SOFT-START AND FAULT MANAGEMENT

Soft-start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amplifier output is also forced low. While the internal 9-μA source charges the SS pin, the error amplifier output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2 V, the fault latch is set and the output pins are driven low. The soft-start cap is then discharged by a 250-μA current sink. No more output pulses are allowed until soft-start is fully discharged and ILIM is below 1.2 V. At this point the fault latch resets and the chip executes a soft-start.

Should the fault latch get set during soft-start, the outputs are immediately terminated, but the soft-start capacitor does not discharge until it has been fully charged first. This results in a controlled hiccup interval for continuous fault conditions.

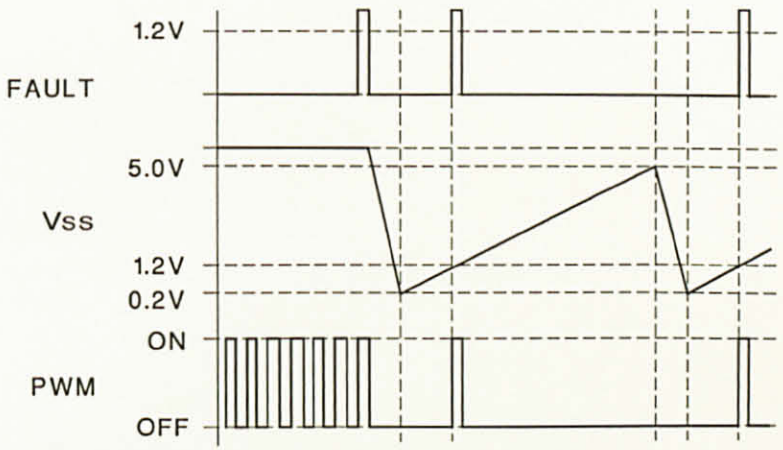


**Figure 5. Soft-Start and Fault Waveforms**

## ACTIVE LOW OUTPUTS DURING UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

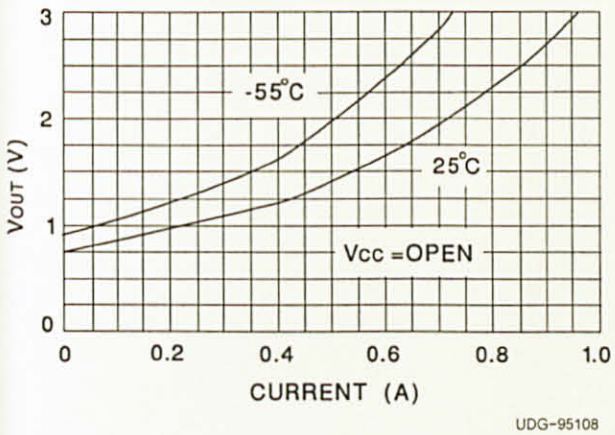


**Figure 6. Output Voltage vs Output Current**

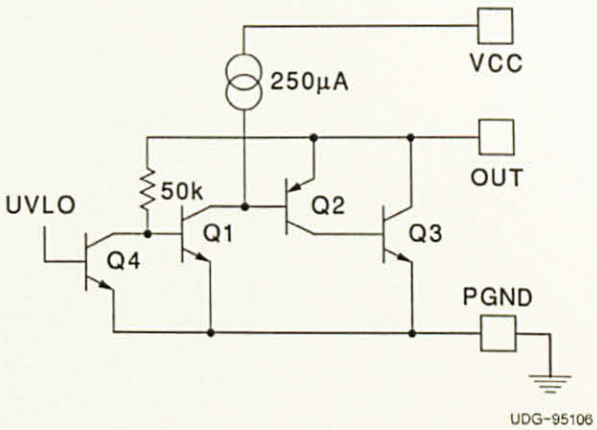


**Figure 7. Output V and I During UVLO**

## CONTROL METHODS

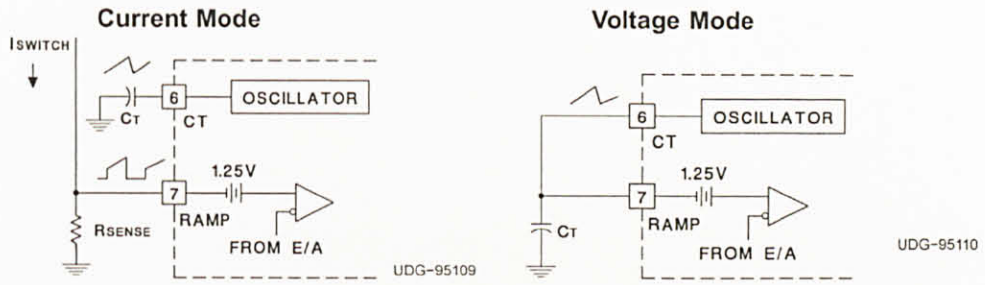


**Figure 8. Control Methods**

## SYNCHRONIZATION

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10 ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that the CLK/LEB pin no longer accepts an incoming synchronizing signal.

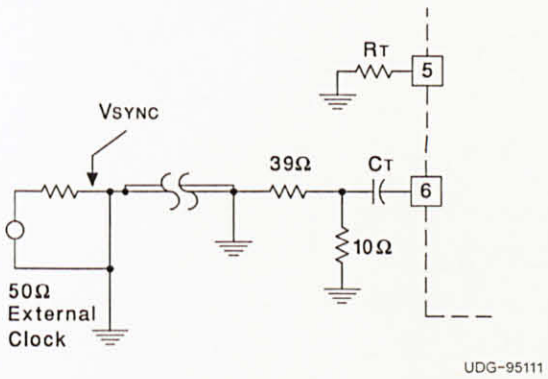


**Figure 9. General Oscillator Synchronization**

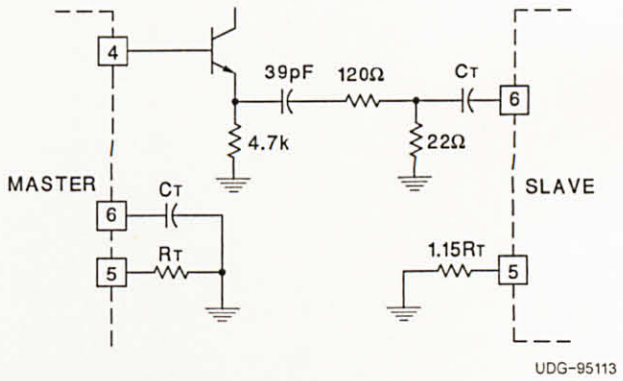


**Figure 10. Two Unit Interface**

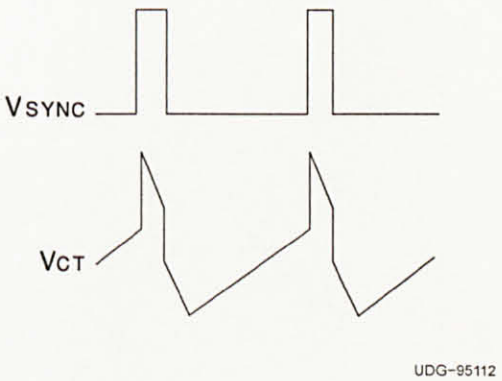


**Figure 11. Operational Waveforms**

## HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A and UC3823AB, UC3825A, and UC3825B can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the device's analog circuitry from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) as shown in the Figure 13 from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

Although they are *single-ended* devices, two output drivers are available on the UC3823A and UC3823B devices. These can be *paralleled* by the use of a 0.5 Ω (noninductive) resistor connected in series with each output for a combined peak current of 4 A.

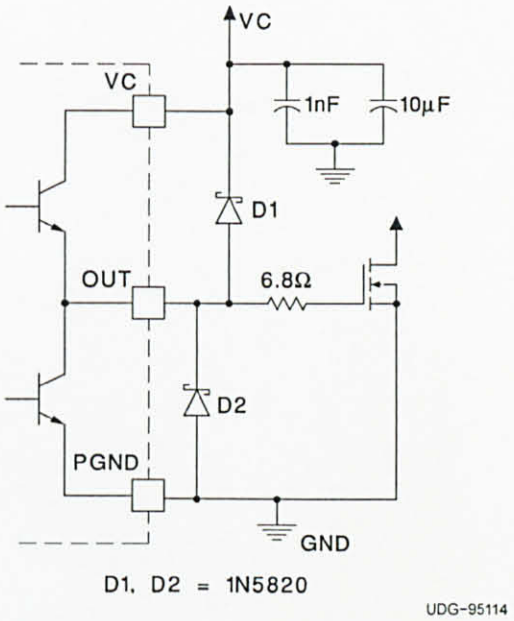


**Figure 12. Power MOSFET Drive Circuit**

## GROUND PLANES

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1-mF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.

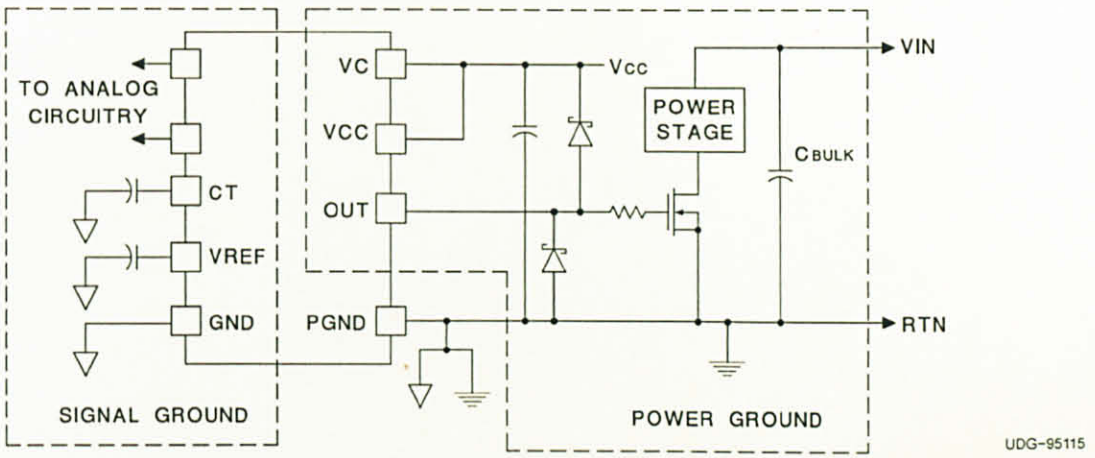


**Figure 13. Ground Planes Diagram**

## OPEN LOOP TEST CIRCUIT

This test fixture is useful for exercising many functions of this device family and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

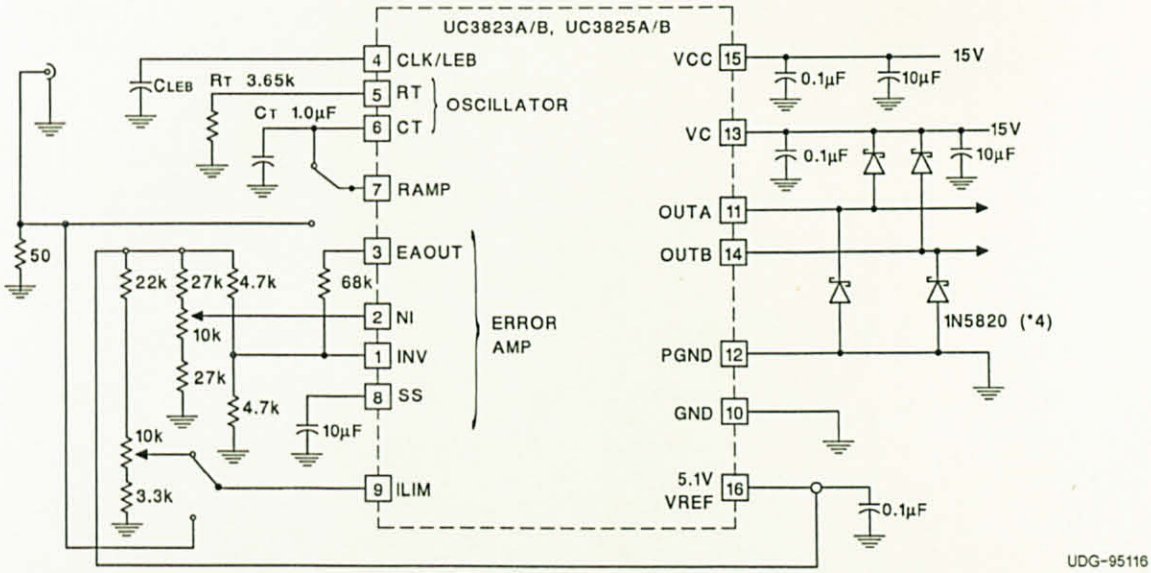


**Figure 14. Open Loop Test Circuit Schematic**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| 5962-87681022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-8768102EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-8768103XA | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | N / A for Pkg Type |
| 5962-89905022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-8990502EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1823AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1823AJ883B | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1823AL | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| UC1823AL883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| UC1823BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1823BJ883B | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1823BL | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1823BL883B | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1825AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1825AJ883B | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1825AL | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| UC1825AL883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| UC1825ALP883B | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | N / A for Pkg Type |
| UC1825BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1825BJ883B | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1825BL/81047 | OBSOLETE | TO/SOT | L | 20 | | TBD | Call TI | Call TI |
| UC1825BL883B | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1825BLP883B | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | N / A for Pkg Type |
| UC2823ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2823ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2823AQ | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC2823AQG3 | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC2823BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC2823BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & | CU NIPDAU | N / A for Pkg Type |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| | | | | | | no Sb/Br) | | |
| UC3825ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3825ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3825AQ | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC3825AQG3 | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC3825BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BDWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BDWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3825BNG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1823A, UC1823B, UC1825A, UC1825B, UC2825A, UC3823A, UC3823B, UC3825A, UC3825B :**

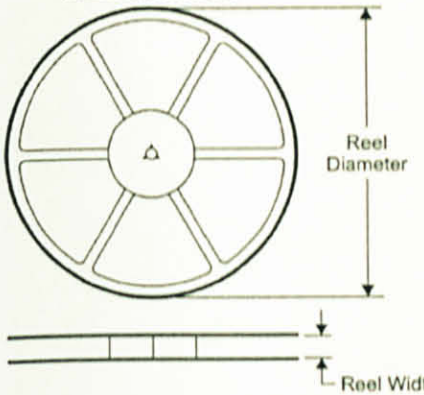
- Automotive: UC2825A-Q1
- Enhanced Product: UC2825A-EP
- Space: UC1823A-SP, UC1825A-SP

NOTE: Qualified Version Definitions:

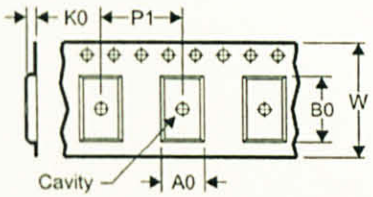
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

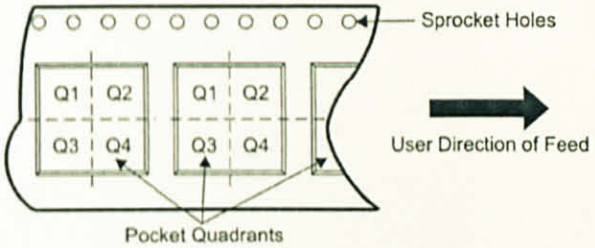



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

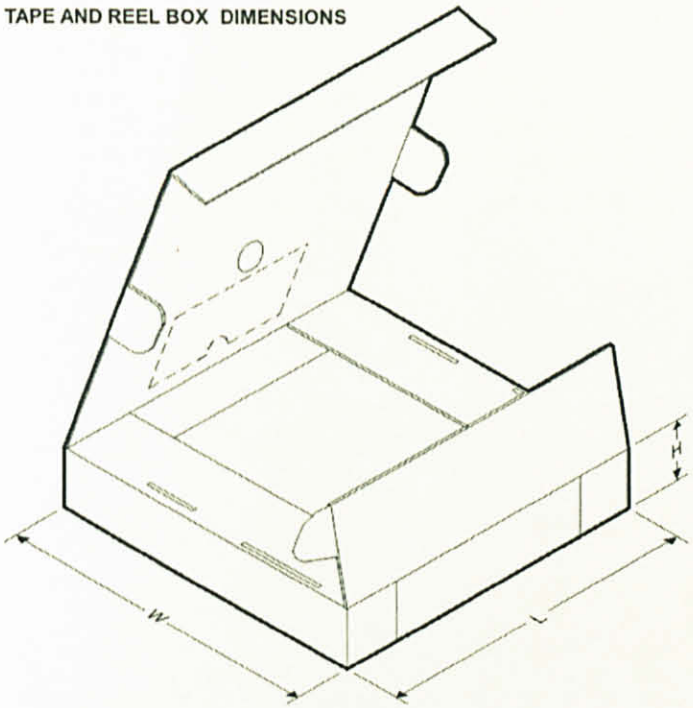
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2823ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC2825ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3823ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3823BDWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3825ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3825BDWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC2823ADWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC2825ADWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC3823ADWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC3823BDWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC3825ADWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC3825BDWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |

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# APPENDIX D

# UC3823A HIGH-SPEED PWM CONTROLLER DATA SHEET



# HIGH-SPEED PWM CONTROLLER

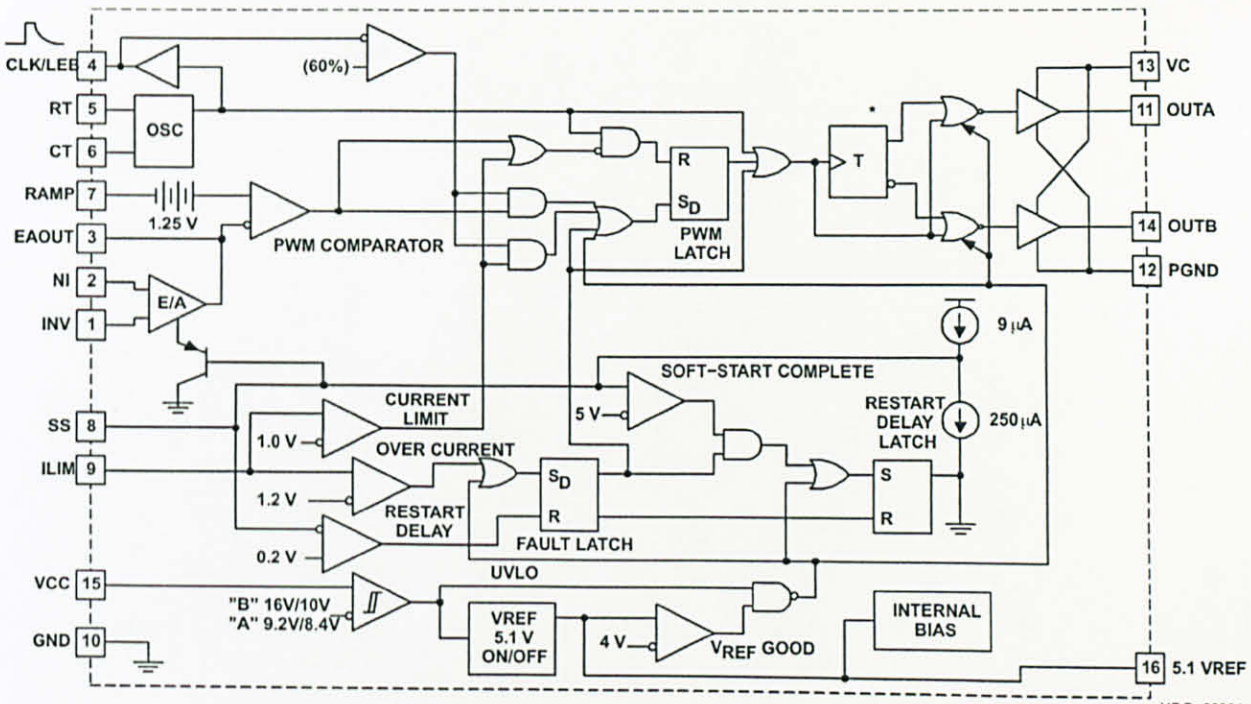
## FEATURES

- Improved Versions of the UC3823/UC3825 PWMs
- Compatible with Voltage-Mode or Current-Mode Control Methods
- Practical Operation at Switching Frequencies to 1 MHz
- 50-ns Propagation Delay to Output
- High-Current Dual Totem Pole Outputs (2-A Peak)
- Trimmed Oscillator Discharge Current
- Low 100-μA Startup Current
- Pulse-by-Pulse Current Limiting Comparator
- Latched Overcurrent Comparator With Full Cycle Restart

## DESCRIPTION

The UC3823A and UC3823B and the UC3825A and UC3825B family of PWM controllers are improved versions of the standard UC3823 and UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset voltage is 2 mV. Current limit threshold is assured to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100 μA, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2-A peak currents during transitions.

## BLOCK DIAGRAM




* On the UC1823A version, toggles Q and $\overline{Q}$ are always low.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2 V. The overcurrent comparator sets a latch that ensures full discharge of the soft-start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft-start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 CLOCK pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC3825A and UC3825B have dual alternating outputs and the same pin configuration of the UC3825. The UC3823A and UC3823B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the UC3823A and UC3823B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. "A" version parts have UVLO thresholds identical to the original UC3823 and UC3825. The "B" versions have UVLO thresholds of 16 V and 10 V, intended for ease of use in off-line applications.

Consult the application note, *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers*, (SLUA125) for detailed technical and applications information.

## ORDERING INFORMATION

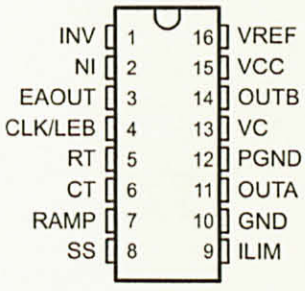
| $T_A$ | MAXIMUM DUTY CYCLE | UVLO | | | | | |
|---|---|---|---|---|---|---|---|
| | | 9.2 V / 8.4 V | | | 16 V / 10 V | | |
| | | SOIC-16[1] (DW) | PDIP-16 (N) | PLCC-20[1] (Q) | SOIC-16 (DW) | PDIP-16 (N) | PLCC-20[1] (Q) |
| −40°C to 85°C | < 100% | UC2823ADW | UC2823AN | UC2823AQ | UC2823BDW | UC2823BN | – |
| | < 50% | UC2825ADW | UC2825AN | UC2825AQ | UC2825BDW | UC2825BN | – |
| −0°C to 70°C | < 100% | UC3823ADW | UC3823AN | UC3823AQ | UC3823BDW | UC3823BN | – |
| | < 50% | UC3825ADW | UC3825AN | UC3825AQ | UC3825BDW | UC3825BN | UC3825BQ |

(1) The DW and Q packages are also available taped and reeled. Add TR suffix to the device type (i.e., UC2823ADWR). To order quantities of 1000 devices per reel for the Q package and 2000 devices per reel for the DW package.

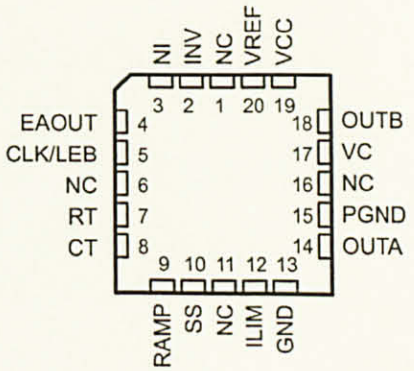
| $T_A$ | MAXIMUM DUTY CYCLE | UVLO | |
|---|---|---|---|
| | | 9.2 V / 8.4 V | |
| | | CDIP-16 (J) | LCCC-20 (L) |
| −55°C to 125°C | < 100% | UC1823AJ, UC1823AJ883B, UC1823AJQMLV | UC1823AL, UC1823AL883B |
| | < 50% | UC1825AJ, UC1825AJ883B, UC1825AJQMLV | UC1825AL, UC1825AL883B, UC1825ALQMLV |

## PIN ASSIGNMENTS

DW, J, OR N PACKAGES
(TOP VIEW)




Q OR L PACKAGES
(TOP VIEW)




NC = no connection

## TERMINAL FUNCTIONS

| TERMINAL | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| | J or DW | Q or L | | |
| CLK/LEB | 4 | 5 | O | Output of the internal oscillator |
| CT | 6 | 8 | I | Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length. |
| EAOUT | 3 | 4 | O | Output of the error amplifier for compensation |
| GND | 10 | 13 | – | Analog ground return pin |
| ILIM | 9 | 12 | I | Input to the current limit comparator |
| INV | 1 | 2 | I | Inverting input to the error amplifier |
| NI | 2 | 3 | I | Non-inverting input to the error amplifier |
| OUTA | 11 | 14 | O | High current totem pole output A of the on-chip drive stage. |
| OUTB | 14 | 18 | O | High current totem pole output B of the on-chip drive stage. |
| PGND | 12 | 15 | – | Ground return pin for the output driver stage |
| RAMP | 7 | 9 | I | Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input. |
| RT | 5 | 7 | I | Timing resistor connection pin for oscillator frequency programming |
| SS | 8 | 10 | I | Soft-start input pin which also doubles as the maximum duty cycle clamp. |
| VC | 13 | 17 | – | Power supply pin for the output stage. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths. |
| VCC | 15 | 19 | – | Power supply pin for the device. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths |
| VREF | 16 | 20 | O | 5.1-V reference. For stability, the reference should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane. |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | | UNIT |
|---|---|---|---|
| $V_{IN}$ | Supply voltage, | VC, VCC | 22 V |
| $I_O$ | Source or sink current, DC | OUTA, OUTB | 0.5 A |
| $I_O$ | Source or sink current, pulse (0.5 μs) | OUTA, OUTB | 2.2 A |
| | Analog inputs | INV, NI, RAMP | −0.3 V to 7 V |
| | | ILIM, SS | −0.3 V to 6 V |
| | Power ground | PGND | ±0.2 V |
| | Outputs | OUTA, OUTB limits | PGND −0.3 V to $V_C$ +0.3 V |
| $I_{CLK}$ | Clock output current | CLK/LEB | −5 mA |
| $I_{O(EA)}$ | Error amplifier output current | EAOUT | 5 mA |
| $I_{SS}$ | Soft-start sink current | SS | 20 mA |
| $I_{OSC}$ | Oscillator charging current | RT | −5 mA |
| $T_J$ | Operating virtual junction temperature range | | −55°C to 150°C |
| $T_{stg}$ | Storage temperature | | −65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | −55C°C to 150°C |
| $t_{STG}$ | Storage temperature | | −65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds | | 300°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$T_A$ = −55°C to 125°C for the UC1823A/UC1825A, $T_A$ = −40°C to 85°C for the UC2823x/UC2825x, $T_A$ = 0°C to 70°C for the UC3823x/UC3825x, $R_T$ = 3.65 kΩ, $C_T$ = 1 nF, $V_{CC}$ = 12 V, $T_A$ = $T_J$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **REFERENCE, $V_{REF}$** | | | | | | |
| $V_O$ | Ouput voltage range | $T_J$ = 25°C, $I_O$ = 1 mA | 5.05 | 5.1 | 5.15 | V |
| | Line regulation | 12 V ≤ VCC ≤ 20 V | | 2 | 15 | mV |
| | Load regulation | 1 mA ≤ $I_O$ ≤ 10 mA | | 5 | 20 | mV |
| | Total output variation | Line, load, temperature | 5.03 | | 5.17 | V |
| | Temperature stability(1) | $T_{(min)}$ < $T_A$ < $T_{(max)}$ | | 0.2 | 0.4 | mV/°C |
| | Output noise voltage(1) | 10 Hz < f < 10 kHz | | 50 | | $\mu V_{RMS}$ |
| | Long term stability(1) | $T_J$ = 125°C, 1000 hours | | 5 | 25 | mV |
| | Short circuit current | VREF = 0 V | 30 | 60 | 90 | mA |
| **OSCILLATOR** | | | | | | |
| $f_{OSC}$ | Initial accuracy(1) | $T_J$ = 25°C | 375 | 400 | 425 | kHz |
| | | $R_T$ = 6.6 kΩ, $C_T$ = 220 pF, $T_A$ = 25°C | 0.9 | 1 | 1.1 | MHz |
| | Total variation(1) | Line, temperature | 350 | | 450 | kHz |
| | | $R_T$ = 6.6 kΩ, $C_T$ = 220 pF, | 0.85 | | 1.15 | MHz |
| | Voltage stability | 12 V < VCC < 20 V | | | 1% | |
| | Temperature stability(1) | $T_{(min)}$ < $T_A$ < $T_{(max)}$ | +/− | 5% | | |
| | High-level output voltage, clock | | 3.7 | 4 | | V |
| | Low-level output voltage, clock | | | 0 | 0.2 | V |
| | Ramp peak | | 2.6 | 2.8 | 3 | V |
| | Ramp valley | | 0.7 | 1 | 1.25 | V |
| | Ramp valley-to-peak | | 1.6 | 1.8 | 2 | V |
| $I_{OSC}$ | Oscillator discharge current | $R_T$ = OPEN, $V_{CT}$ = 2 V | 9 | 10 | 11 | mA |
| **ERROR AMPLIFIER** | | | | | | |
| | Input offset voltage | | | 2 | 10 | mV |
| | Input bias current | | | 0.6 | 3 | µA |
| | Input offset current | | | 0.1 | 1 | µA |
| | Open loop gain | 1 V < $V_O$ < 4 V | 60 | 95 | | dB |
| CMRR | Common mode rejection ratio | 1.5 V < $V_{CM}$ < 5.5 V | 75 | 95 | | dB |
| PSRR | Power supply rejection ratio | 12 V < $V_{CC}$ < 20 V | 85 | 110 | | dB |
| $I_{O(sink)}$ | Output sink current | $V_{EAOUT}$ = 1 V | 1 | 2.5 | | mA |
| $I_{O(src)}$ | Output source current | $V_{EAOUT}$ = 4 V | −0.5 | −1.3 | | mA |
| | High-level output voltage | $I_{EAOUT}$ = −0.5 mA | 4.5 | 4.7 | 5 | V |
| | Low-level output voltage | $I_{EAOUT}$ = −1 mA | 0 | 0.5 | 1 | V |
| | Gain bandwidth product | f = 200 kHz | 6 | 12 | | Mhz |
| | Slew rate(1) | | 6 | 9 | | V/µs |

(1) Ensured by design. Not production tested.

## ELECTRICAL CHARACTERISTICS

$T_A$ = −55°C to 125°C for the UC1823A/UC1825A, $T_A$ = −40°C to 85°C for the UC2823x/UC2825x, $T_A$ = 0°C to 70°C for the UC3823x/UC3825x, $R_T$ = 3.65 kΩ, $C_T$ = 1 nF, $V_{CC}$ = 12 V, $T_A$ = $T_J$ (unless otherwise noted)

| | | | | | | |
|---|---|---|---|---|---|---|
| **PWM COMPARATOR** | | | | | | |
| $I_{BIAS}$ | Bias current, RAMP | $V_{RAMP}$ = 0 V | | −1 | −8 | µA |
| | Minimum duty cycle | | | | 0% | |
| | Maximum duty cycle | | 85% | | | |
| $t_{LEB}$ | Leading edge blanking time | $R_{LEB}$ = 2 kΩ, $C_{LEB}$ = 470 pF | 300 | 375 | 450 | ns |
| $R_{LEB}$ | Leading edge blanking resistance | $V_{CLK/LEB}$ = 3 V | 8.5 | 10.0 | 11.5 | kΩ |
| $V_{ZDC}$ | Zero dc threshold voltage, EAOUT | $V_{RAMP}$ = 0 V | 1.10 | 1.25 | 1.4 | V |
| $t_{DELAY}$ | Delay-to-output time | $V_{EAOUT}$ = 2.1 V, $V_{ILIM}$ = 0 V to 2 V step | | 50 | 80 | ns |
| **CURRENT LIMIT / START SEQUENCE / FAULT** | | | | | | |
| $I_{SS}$ | Soft-start charge current | $V_{SS}$= 2.5 V | 8 | 14 | 20 | µA |
| $V_{SS}$ | Full soft-start threshold voltage | | 4.3 | 5 | | V |
| $I_{DSCH}$ | Restart discharge current | $V_{SS}$= 2.5 V | 100 | 250 | 350 | µA |
| $I_{SS}$ | Restart threshold voltage | | | 0.3 | 0.5 | V |
| $I_{BIAS}$ | ILIM bias current | $V_{ILIM}$ = 0 V to 2 V step | | | 15 | µA |
| $I_{CL}$ | Current limit threshold voltage | | 0.95 | 1 | 1.05 | V |
| | Overcurrent threshold voltage | | 1.14 | 1.2 | 1.26 | |
| $t_d$ | Delay-to-output time, ILIM(1) | $V_{ILIM}$ = 0 V to 2 V step | | 50 | 80 | ns |
| **OUTPUT** | | | | | | |
| | Low-level output saturation voltage | $I_{OUT}$ = 20 mA | | 0.25 | 0.4 | V |
| | | $I_{OUT}$ = 200 mA | | 1.2 | 2.2 | |
| | High-level output saturation voltage | $I_{OUT}$ = 20 mA | | 1.9 | 2.9 | |
| | | $I_{OUT}$ = 200 mA | | 2 | 3 | |
| $t_r$, $t_f$ | Rise/fall time(1) | $C_L$ = 1 nF | | 20 | 45 | ns |
| **UNDERVOLTAGE LOCKOUT (UVLO)** | | | | | | |
| | Start threshold voltage | UC2823B, UC2825B, UC3825B, UC3825B | | 16 | 17 | V |
| | | UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A | 8.4 | 9.2 | 9.6 | |
| | Stop threshold voltage | UC2823B, UC2825B, UC3825B, UC3825B | 9 | 10 | | |
| | OVLO hysteresis | UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A | 0.4 | 0.8 | 1.2 | |
| | | UC2823B, UC2825B, UC3825B, UC3825B | 5 | 6 | 7 | |
| **SUPPLY CURRENT** | | | | | | |
| $I_{su}$ | Startup current | VC = VCC = $V_{TH}$ = −0.5 V | | 100 | 300 | µA |
| $I_{CC}$ | Input current | | | 28 | 36 | mA |

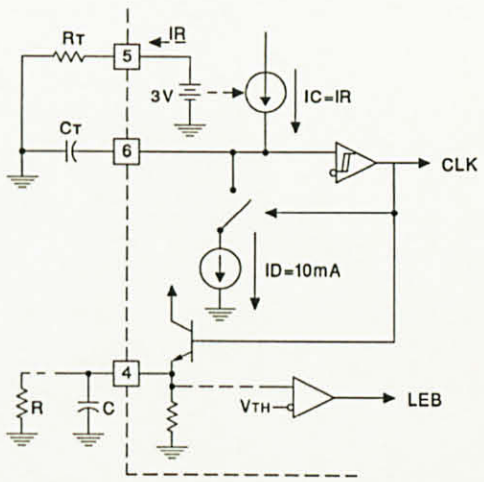
(1) Ensured by design. Not production tested.

## APPLICATION INFORMATION

The oscillator of the UC3823A, UC3823B, UC3825A, and UC3825B is a saw tooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin ($C_{CT}$). The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency (RT) and $D_{MAX}$. The design equations are:

$$R_T = \frac{3\ V}{(10\ mA) \times (1 - D_{MAX})} \qquad C_T = \frac{(1.6 \times D_{MAX})}{(R_T \times f)} \tag{1}$$

Recommended values for $R_T$ range from 1 kΩ to 100 kΩ. Control of $D_{MAX}$ less than 70% is not recommended.




UDG-95102

**Figure 1. Oscillator**

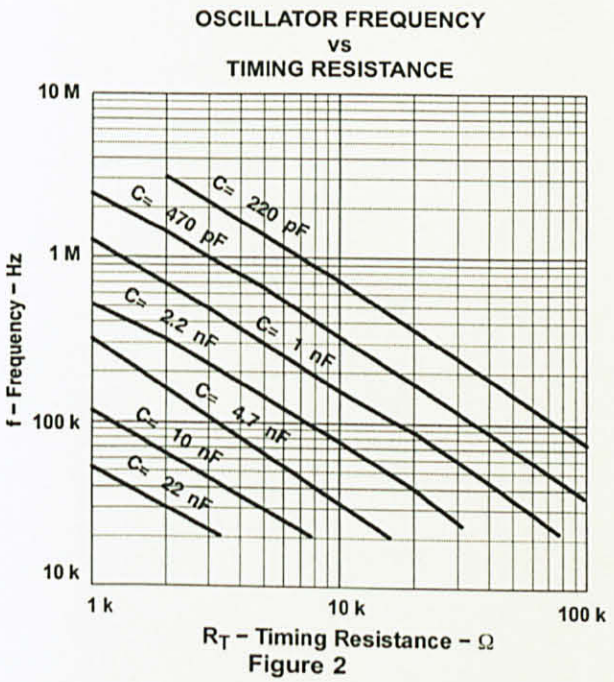



**Figure 2**

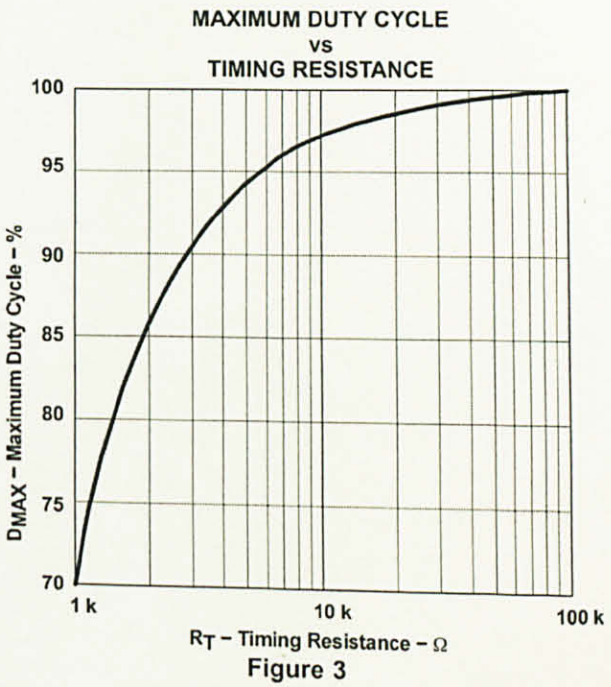



**Figure 3**

## LEADING EDGE BLANKING

The UC3823A, UC2823B, UC3825A, and UC3825B perform fixed frequency pulse width modulation control. The UC3823A, and UC3823B outputs operate together at the switching frequency and can vary from zero to some value less than 100%. The UC3825A and UC3825B outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

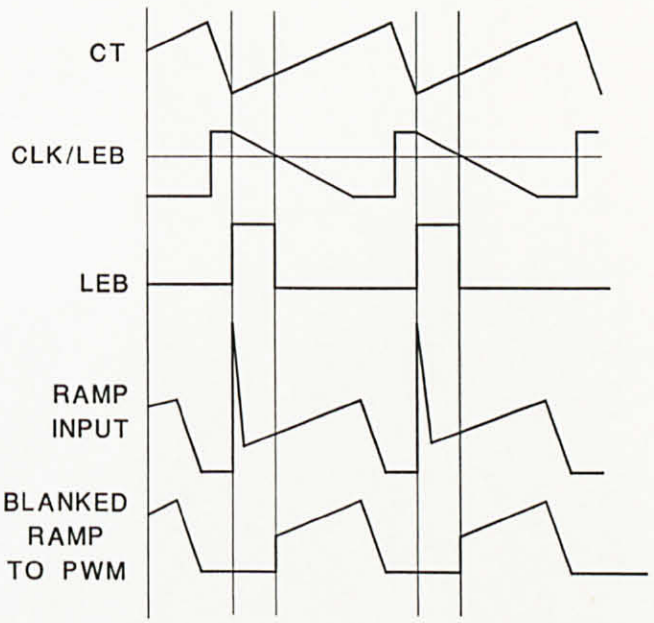
Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a leading edge blanking (LEB) period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-kΩ resistor determines the blanked interval. The 10-kΩ resistor has a 10% tolerance. For more accuracy, an external 2-kΩ 1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 kΩ with a tolerance of 2.4%. The design equation is:

$$t_{LEB} = 0.5 \times (R \parallel 10\ k\Omega) \times C \quad (2)$$

Values of R less than 2 kΩ should not be used.

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.




UDG-95105

**Figure 4. Leading Edge Blanking Operational Waveforms**

## UVLO, SOFT-START AND FAULT MANAGEMENT

Soft-start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amplifier output is also forced low. While the internal 9-µA source charges the SS pin, the error amplifier output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2 V, the fault latch is set and the output pins are driven low. The soft-start cap is then discharged by a 250-µA current sink. No more output pulses are allowed until soft-start is fully discharged and ILIM is below 1.2 V. At this point the fault latch resets and the chip executes a soft-start.

Should the fault latch get set during soft-start, the outputs are immediately terminated, but the soft-start capacitor does not discharge until it has been fully charged first. This results in a controlled hiccup interval for continuous fault conditions.

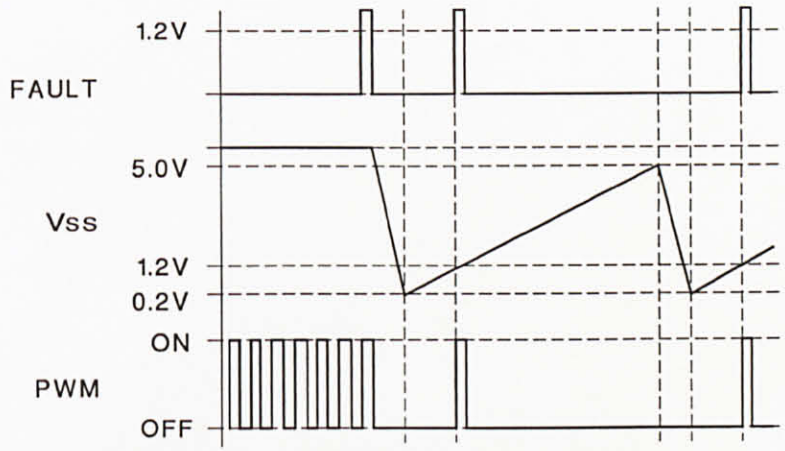



**Figure 5. Soft-Start and Fault Waveforms**

## ACTIVE LOW OUTPUTS DURING UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

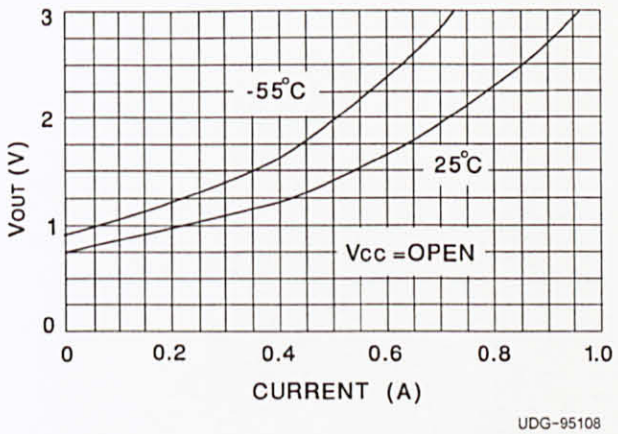



**Figure 6. Output Voltage vs Output Current**

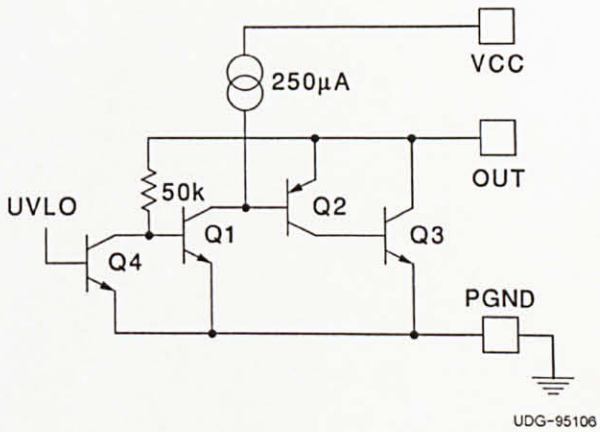



**Figure 7. Output V and I During UVLO**

## CONTROL METHODS

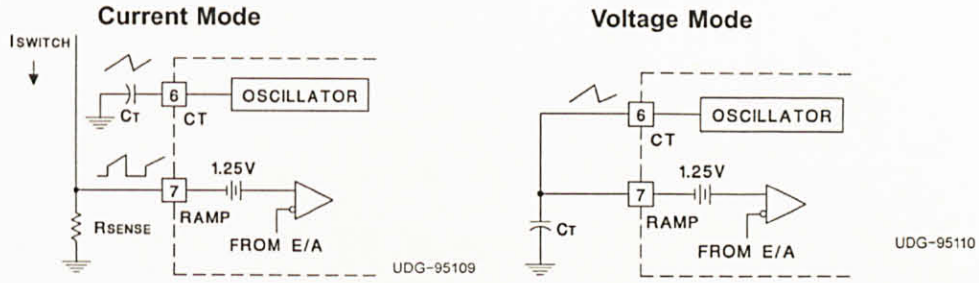



**Figure 8. Control Methods**

## SYNCHRONIZATION

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10 ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that the CLK/LEB pin no longer accepts an incoming synchronizing signal.

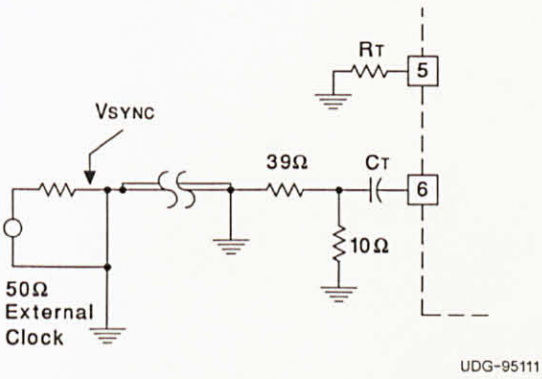



**Figure 9. General Oscillator Synchronization**

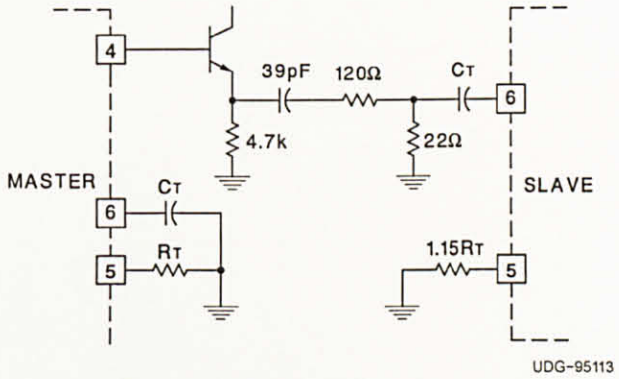



**Figure 10. Two Unit Interface**

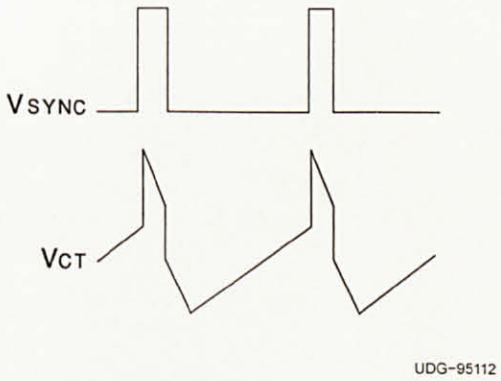



**Figure 11. Operational Waveforms**

## HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A and UC3823AB, UC3825A, and UC3825B can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the device's analog circuitry from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) as shown in the Figure 13 from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

Although they are *single-ended* devices, two output drivers are available on the UC3823A and UC3823B devices. These can be *paralleled* by the use of a 0.5 Ω (noninductive) resistor connected in series with each output for a combined peak current of 4 A.

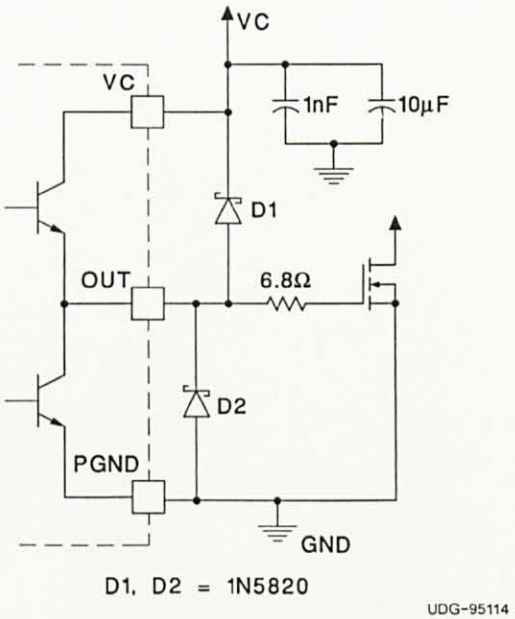



**Figure 12. Power MOSFET Drive Circuit**

## GROUND PLANES

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1-mF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.

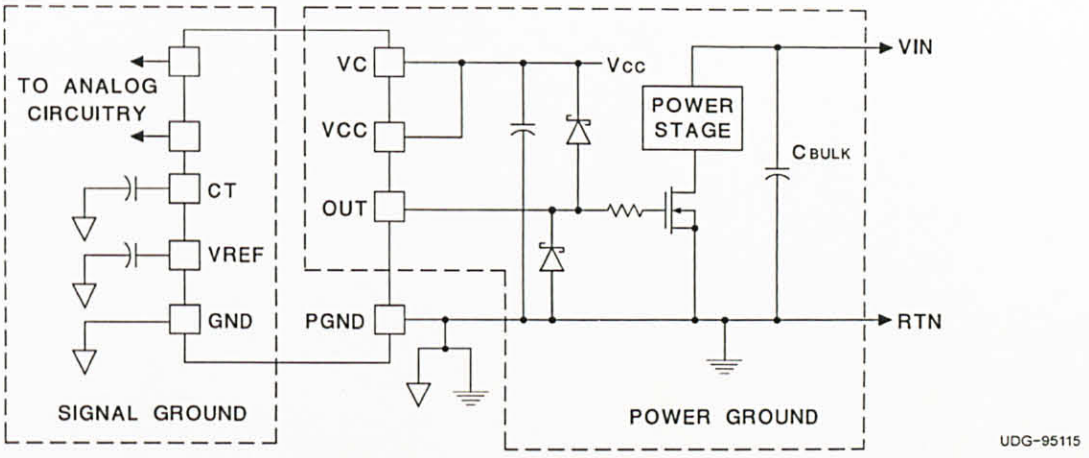



**Figure 13. Ground Planes Diagram**

## OPEN LOOP TEST CIRCUIT

This test fixture is useful for exercising many functions of this device family and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

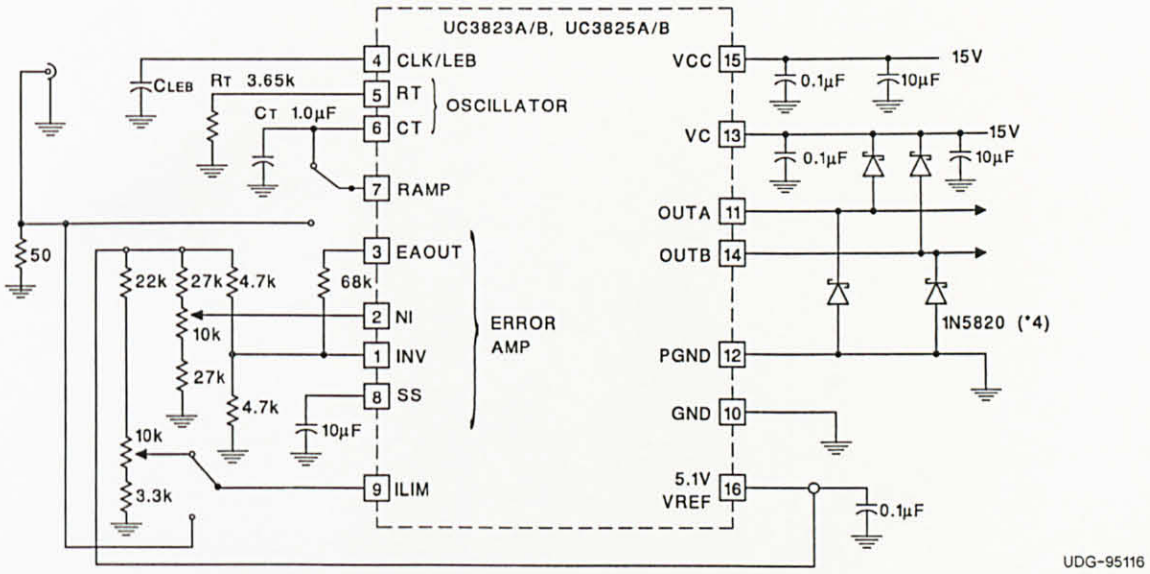



**Figure 14. Open Loop Test Circuit Schematic**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 5962-87681022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-8768102EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-8768103XA | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | N / A for Pkg Type |
| 5962-89905022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-8990502EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1823AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1823AJ883B | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1823AL | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| UC1823AL883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| UC1823BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1823BJ883B | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1823BL | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1823BL883B | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1825AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1825AJ883B | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| UC1825AL | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| UC1825AL883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| UC1825ALP883B | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | N / A for Pkg Type |
| UC1825BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1825BJ883B | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1825BL/81047 | OBSOLETE | TO/SOT | L | 20 | | TBD | Call TI | Call TI |
| UC1825BL883B | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1825BLP883B | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | N / A for Pkg Type |
| UC2823ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2823ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2823AQ | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC2823AQG3 | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC2823BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC2823BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & | CU NIPDAU | N / A for Pkg Type |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| | | | | | | no Sb/Br) | | |
| UC2823BNG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2825ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2825ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2825AQ | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC2825AQG3 | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC2825BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC2825BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2825BNG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3823ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3823ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3823BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823BDWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823BDWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3823BNG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & | CU NIPDAU | N / A for Pkg Type |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| | | | | | | no Sb/Br) | | |
| UC3825ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3825ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3825AQ | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC3825AQG3 | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC3825BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BDWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BDWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3825BNG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1823A, UC1823B, UC1825A, UC1825B, UC2825A, UC3823A, UC3823B, UC3825A, UC3825B :**

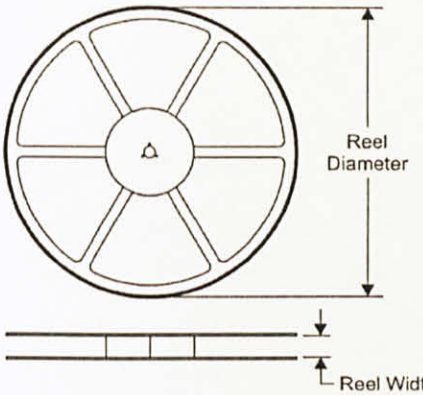
- Automotive: UC2825A-Q1
- Enhanced Product: UC2825A-EP
- Space: UC1823A-SP, UC1825A-SP

NOTE: Qualified Version Definitions:

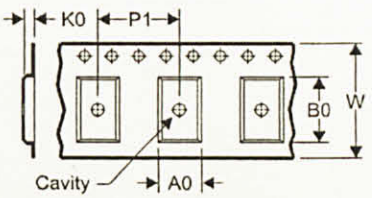
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

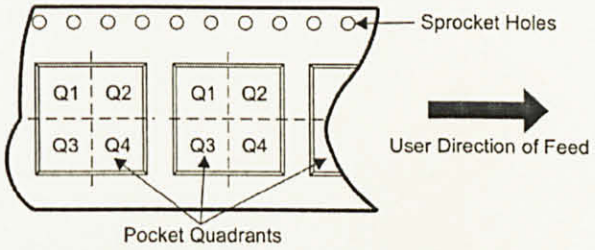



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

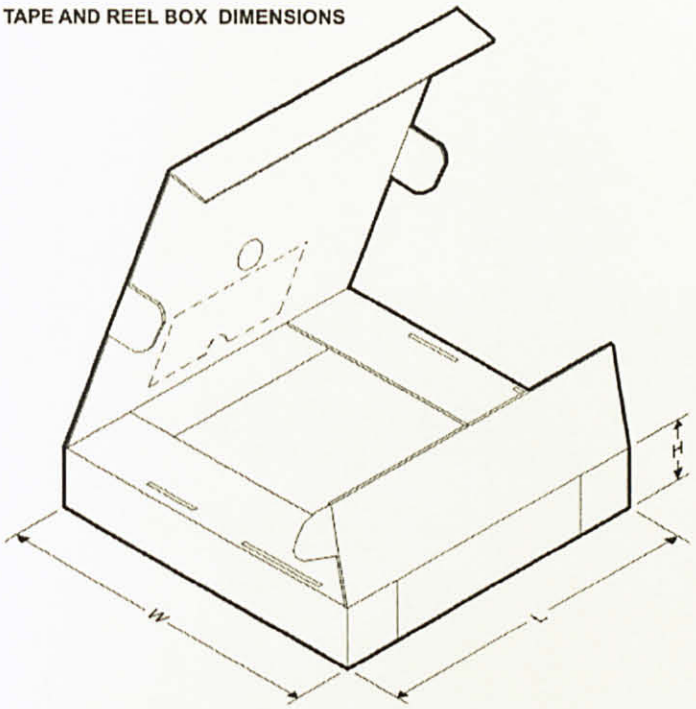
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2823ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC2825ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3823ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3823BDWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3825ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3825BDWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.85 | 10.8 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC2823ADWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC2825ADWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC3823ADWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC3823BDWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC3825ADWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| UC3825BDWTR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |

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| Power Mgmt | power.ti.com | Security | www.ti.com/security |
| Microcontrollers | microcontroller.ti.com | Telephony | www.ti.com/telephony |
| RFID | www.ti-rfid.com | Video & Imaging | www.ti.com/video |
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# APPENDIX E

## SG3526 PULSE WIDTH MODULATION CONTROL CIRCUIT DATA SHEET

# SG3526

# Pulse Width Modulation Control Circuit

The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B–series CMOS compatible. Active low logic design allows easy wired–OR connections for maximum flexibility. The versatility of this device enables implementation in single–ended or push–pull switching regulators that are transformerless or transformer coupled. The SG3526 is specified over a junction temperature range of 0° to +125°C.

- 8.0 V to 35 V Operation
- 5.0 V ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft–Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

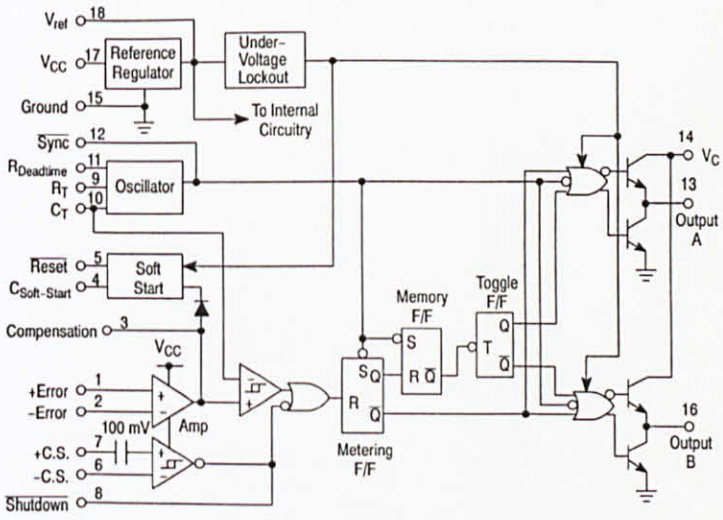


**Figure 1. Representative Block Diagram**

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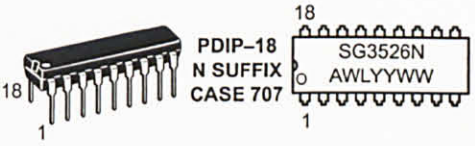
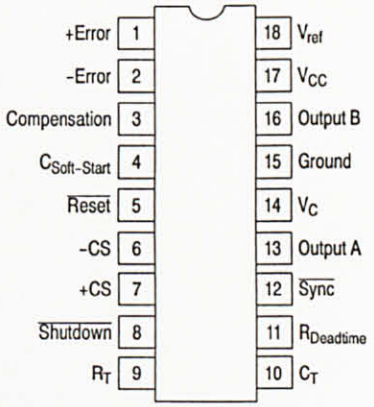
**MARKING DIAGRAM**




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| SG3526N | PDIP–18 | 20 Units/Rail |

**MAXIMUM RATINGS** (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | +40 | Vdc |
| Collector Supply Voltage | $V_C$ | +40 | Vdc |
| Logic Inputs | | –0.3 to +5.5 | V |
| Analog Inputs | | –0.3 to $V_{CC}$ | V |
| Output Current, Source or Sink | $I_O$ | ±200 | mA |
| Reference Load Current ($V_{CC}$ = 40 V, Note 2.) | $I_{ref}$ | 50 | mA |
| Logic Sink Current | | 15 | mA |
| Power Dissipation<br>$T_A$ = +25°C (Note 3.)<br>$T_C$ = +25°C (Note 4.) | $P_D$ | <br>1000<br>3000 | mW |
| Thermal Resistance Junction–to–Air | $R_{\theta JA}$ | 100 | °C/W |
| Thermal Resistance Junction–to–Case | $R_{\theta JC}$ | 42 | °C/W |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Lead Temperature (Soldering, 10 Seconds) | $T_{Solder}$ | ±300 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 8.0 | 35 | Vdc |
| Collector Supply Voltage | $V_C$ | 4.5 | 35 | Vdc |
| Output Sink/Source Current (Each Output) | $I_O$ | 0 | ±100 | mA |
| Reference Load Current | $I_{ref}$ | 0 | 20 | mA |
| Oscillator Frequency Range | $f_{osc}$ | 0.001 | 400 | kHz |
| Oscillator Timing Resistor | $R_T$ | 2.0 | 150 | kΩ |
| Oscillator Timing Capacitor | $C_T$ | 0.001 | 20 | μF |
| Available Deadtime Range (40 kHz) | – | 3.0 | 50 | % |
| Operating Junction Temperature Range | $T_J$ | 0 | +125 | °C |

1. Values beyond which damage may occur.
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above +50°C.
4. Derate at 24 mW/°C for case temperatures above +25°C.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 Vdc, $T_J$ = $T_{low}$ to $T_{high}$ [Note 6.], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **REFERENCE SECTION** (Note 7.) | | | | | |
| Reference Output Voltage ($T_J$ = +25°C) | $V_{ref}$ | 4.90 | 5.00 | 5.10 | V |
| Line Regulation (+8.0 V ≤ $V_{CC}$ ≤ +35 V) | $Reg_{line}$ | – | 10 | 30 | mV |
| Load Regulation (0 mA ≤ $I_L$ ≤ 20 mA) | $Reg_{load}$ | – | 10 | 50 | mV |
| Temperature Stability | $\Delta V_{ref}/\Delta T$ | – | 10 | – | mV |
| Total Reference Output Voltage Variation (+8.0 V ≤ $V_{CC}$ ≤ +35 V, 0 mA ≤ $I_L$ ≤ 20 mA) | $\Delta V_{ref}$ | 4.85 | 5.00 | 5.15 | V |
| Short Circuit Current ($V_{ref}$ = 0 V) (Note 5.) | $I_{SC}$ | 25 | 80 | 125 | mA |
| **UNDERVOLTAGE LOCKOUT** | | | | | |
| $\overline{Reset}$ Output Voltage ($V_{ref}$ = +3.8 V) | | – | 0.2 | 0.4 | V |
| $\overline{Reset}$ Output Voltage ($V_{ref}$ = +4.8 V) | | 2.4 | 4.8 | – | V |
| **OSCILLATOR SECTION** (Note 8.) | | | | | |
| Initial Accuracy ($T_J$ = +25°C) | | – | ±3.0 | ±8.0 | % |
| Frequency Stability over Power Supply Range (+8.0 V ≤ $V_{CC}$ ≤ +35 V) | $\frac{\Delta f_{osc}}{\Delta V_{CC}}$ | – | 0.5 | 1.0 | % |
| Frequency Stability over Temperature ($\Delta T_J$ = $T_{low}$ to $T_{high}$) | $\frac{\Delta f_{osc}}{\Delta T_J}$ | – | 2.0 | – | % |
| Minimum Frequency ($R_T$ = 150 kΩ, $C_T$ = 20 μF) | $f_{min}$ | – | 0.5 | – | Hz |
| Maximum Frequency ($R_T$ = 2.0 kΩ, $C_T$ = 0.001 μF) | $f_{max}$ | 400 | – | – | kHz |
| Sawtooth Peak Voltage ($V_{CC}$ = +35 V) | $V_{osc}(P)$ | – | 3.0 | 3.5 | V |
| Sawtooth Valley Voltage ($V_{CC}$ = +8.0 V) | $V_{osc}(V)$ | 0.45 | 0.8 | – | V |
| **ERROR AMPLIFIER SECTION** (Note 9.) | | | | | |
| Input Offset Voltage ($R_S$ ≤ 2.0 kΩ) | $V_{IO}$ | – | 2.0 | 10 | mV |
| Input Bias Current | $I_{IB}$ | – | –350 | –2000 | nA |
| Input Offset Current | $I_{IO}$ | – | 35 | 200 | nA |
| DC Open Loop Gain ($R_L$ ≥ 10 MΩ) | $A_{VOL}$ | 60 | 72 | – | dB |
| High Output Voltage ($V_{Pin\ 1}$–$V_{Pin\ 2}$ ≥ +150 mV, $I_{source}$ = 100 μA) | $V_{OH}$ | 3.6 | 4.2 | – | V |
| Low Output Voltage ($V_{Pin\ 2}$–$V_{Pin\ 1}$ ≥ +150 mV, $I_{sink}$ = 100 μA) | $V_{OL}$ | – | 0.2 | 0.4 | V |
| Common Mode Rejection Ratio ($R_S$ ≤ 2.0 kΩ) | CMRR | 70 | 94 | – | dB |
| Power Supply Rejection Ratio (+12 V ≤ $V_{CC}$ ≤ +18 V) | PSRR | 66 | 80 | – | dB |

5. Maximum junction temperature must be observed.
6. $T_{low}$ = 0°C $T_{high}$ = +125°C
7. $I_L$ = 0 mA unless otherwise noted.
8. $f_{osc}$ = 40 kHz ($R_T$ = 4.12 kΩ ± 1%, $C_T$ = 0.01 μF ± 1%, $R_D$ = 0 Ω)
9. 0 V ≤ $V_{CM}$ ≤ +5.2 V.

**ELECTRICAL CHARACTERISTICS (continued)**

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **PWM COMPARATOR SECTION** (Note 10.) | | | | | |
| Minimum Duty Cycle ($V_{Compensation}$ = +0.4 V) | $DC_{min}$ | – | – | 0 | % |
| Maximum Duty Cycle ($V_{Compensation}$ = +3.6 V) | $DC_{max}$ | 45 | 49 | – | % |
| **DIGITAL PORTS (SYNC, SHUTDOWN, RESET)** | | | | | |
| Output Voltage | | | | | V |
| (High Logic Level) ($I_{source}$ = 40 μA) | $V_{OH}$ | 2.4 | 4.0 | – | |
| (Low Logic Level) ($I_{sink}$ = 3.6 mA) | $V_{OL}$ | – | 0.2 | 0.4 | |
| Input Current — High Logic Level | | | | | μA |
| (High Logic Level) ($V_{IH}$ = +2.4 V) | $I_{IH}$ | – | –125 | –200 | |
| (Low Logic Level) ($V_{IL}$ = +0.4 V) | $I_{IL}$ | – | –225 | –360 | |
| **CURRENT LIMIT COMPARATOR SECTION** (Note 12.) | | | | | |
| Sense Voltage ($R_S \leq 50\ \Omega$) | $V_{sense}$ | 80 | 100 | 120 | mV |
| Input Bias Current | $I_{IB}$ | – | –3.0 | –10 | μA |
| **SOFT–START SECTION** | | | | | |
| Error Clamp Voltage ($\overline{Reset}$ = +0.4 V) | | – | 0.1 | 0.4 | V |
| $C_{Soft-Start}$ Charging Current ($\overline{Reset}$ = +2.4 V) | $I_{CS}$ | 50 | 100 | 150 | μA |
| **OUTPUT DRIVERS** (Each Output, $V_C$ = +15 Vdc, unless otherwise noted.) | | | | | |
| Output High Level | $V_{OH}$ | | | | V |
| $I_{source}$ = 20 mA | | 12.5 | 13.5 | – | |
| $I_{source}$ = 100 mA | | 12 | 13 | – | |
| Output Low Level | $V_{OL}$ | | | | V |
| $I_{sink}$ = 20 mA | | – | 0.2 | 0.3 | |
| $I_{sink}$ = 100 mA | | – | 1.2 | 2.0 | |
| Collector Leakage, $V_C$ = +40 V | $I_{C(leak)}$ | – | 50 | 150 | μA |
| Rise Time ($C_L$ = 1000 pF) | $t_r$ | – | 0.3 | 0.6 | μs |
| Fall Time ($C_L$ = 1000 pF) | $t_f$ | – | 0.1 | 0.2 | μs |
| Supply Current ($\overline{Shutdown}$ = +0.4 V, $V_{CC}$ = +35 V, $R_T$ = 4.12 kΩ) | $I_{CC}$ | – | 18 | 30 | mA |

10. $f_{osc}$ = 40 kHz ($R_T$ = 4.12 kΩ ± 1%, $C_T$ = 0.01 μF ± 1%, $R_D$ = 0 Ω)
11. $0\ V \leq V_{CM} \leq +5.2\ V$
12. $0\ V \leq V_{CM} \leq +12\ V$

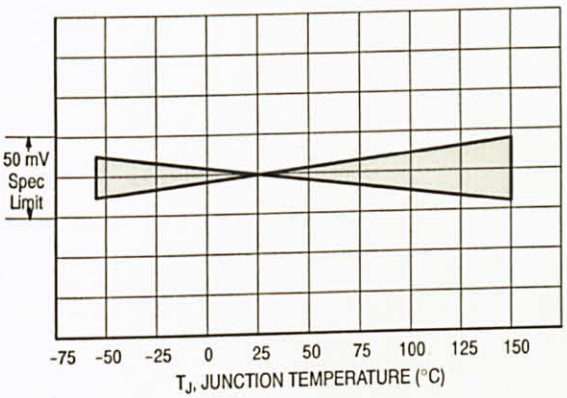



Figure 2. Reference Stability over Temperature

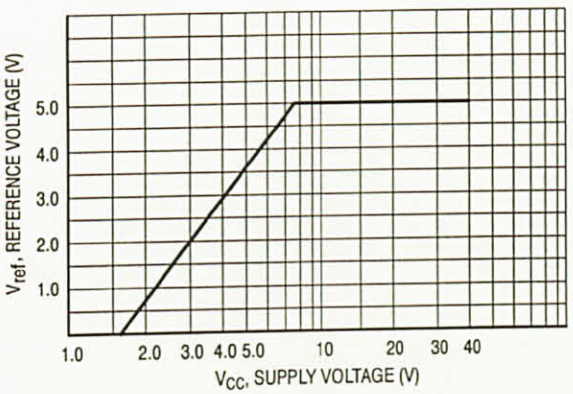



Figure 3. Reference Voltage as a Function Supply Voltage

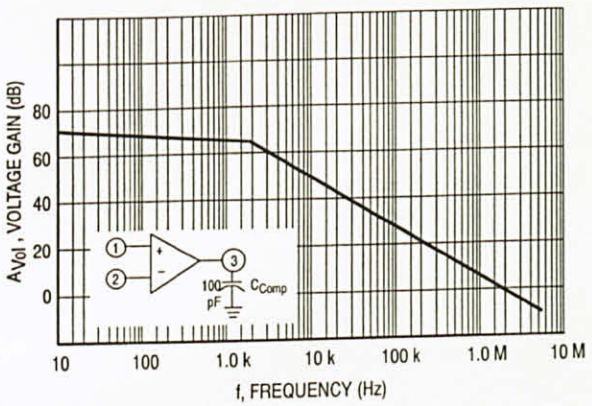



Figure 4. Error Amplifier Open Loop Frequency Response

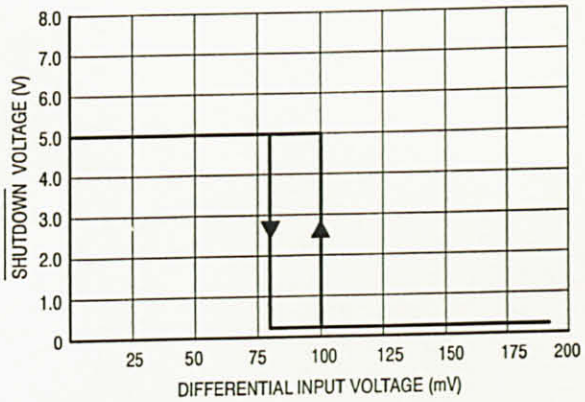



Figure 5. Current Limit Comparator Threshold

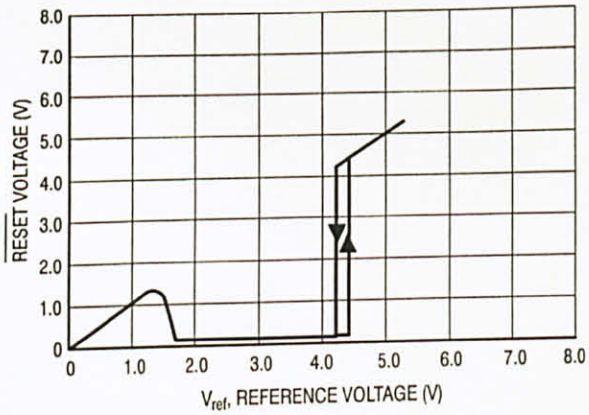



Figure 6. Undervoltage Lockout Characteristic

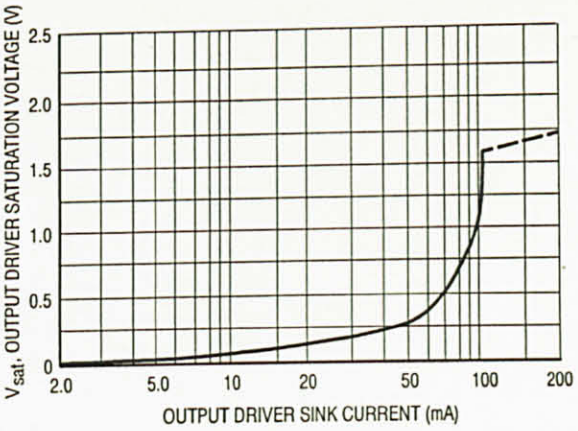



Figure 7. Output Driver Saturation Voltage as a Function of Sink Current

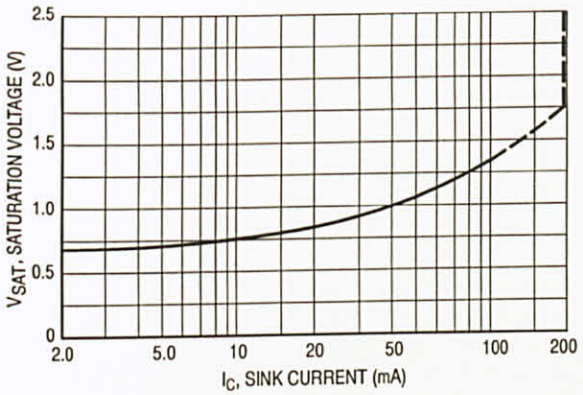



Figure 8. $V_C$ Saturation Voltage as a Function of Sink Current

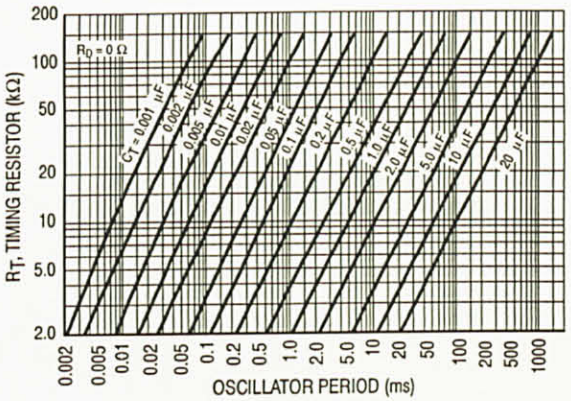



Figure 9. Oscillator Period

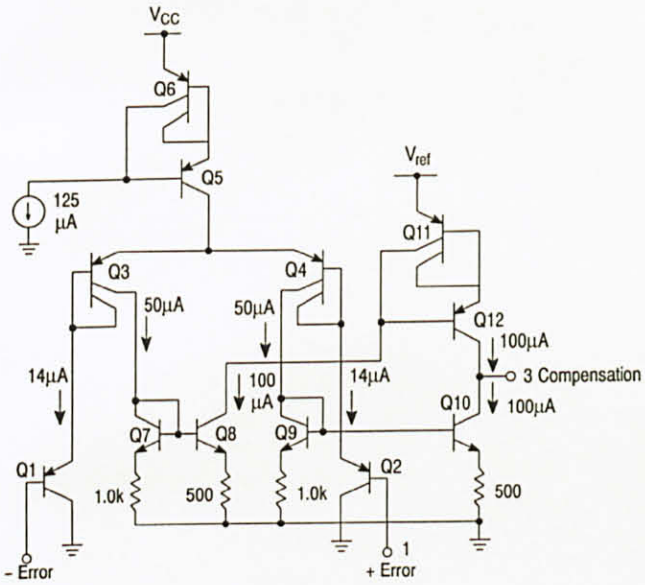



Figure 10. Error Amplifier

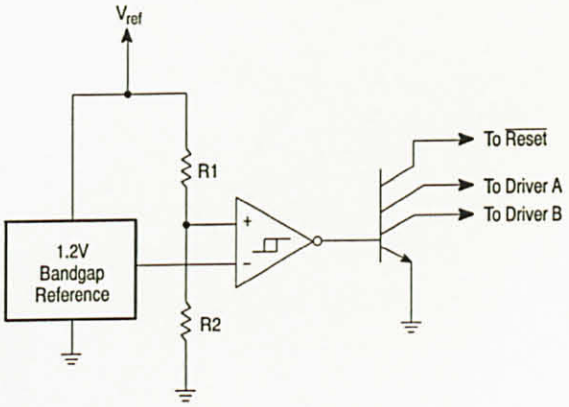
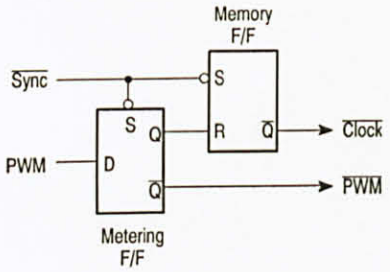



Figure 11. Undervoltage Lockout

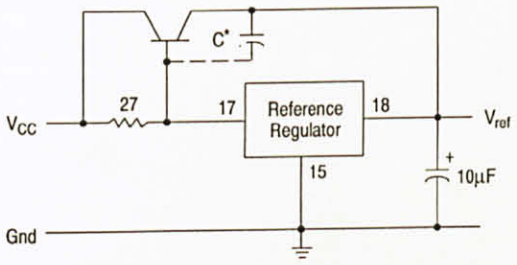



The metering Flip-Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip-Flop prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

Figure 12. Pulse Processing Logic

## APPLICATIONS INFORMATION




* May be required with some types of transistors

**Figure 13. Extending Reference Output Current Capability**

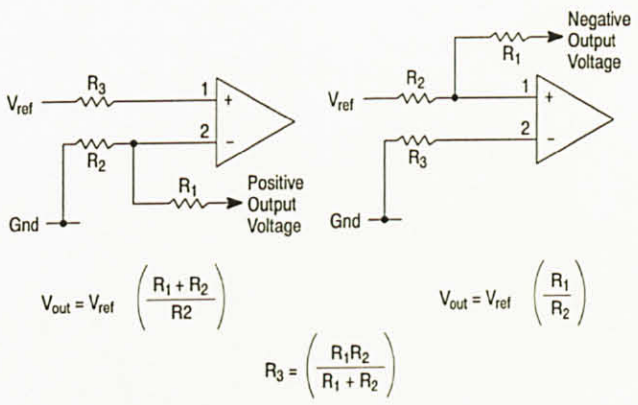



**Figure 14. Error Amplifier Connections**

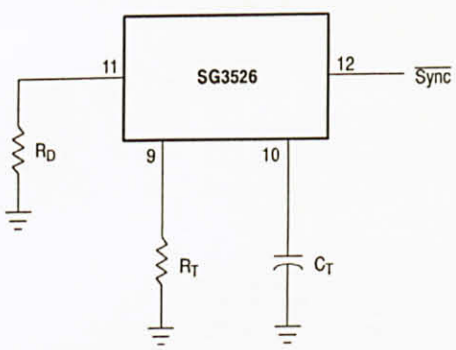



**Figure 15. Oscillator Connections**

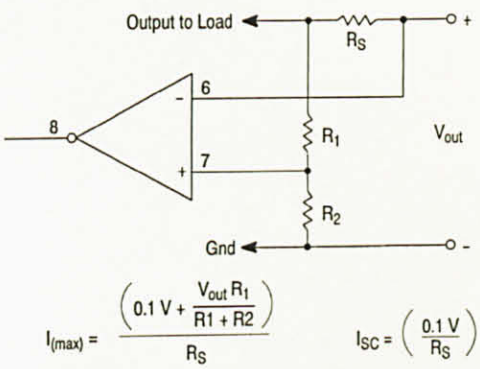



**Figure 16. Foldback Current Limiting**

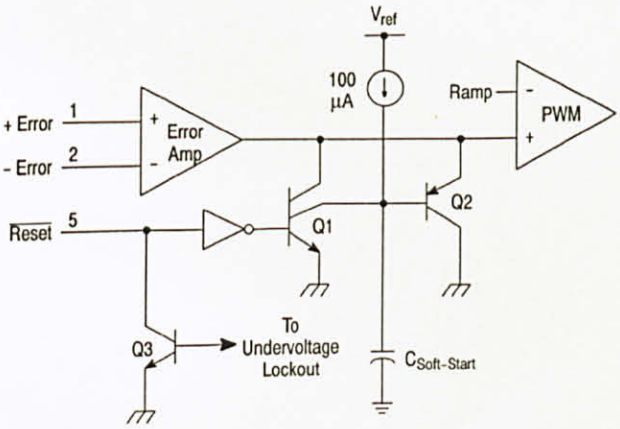
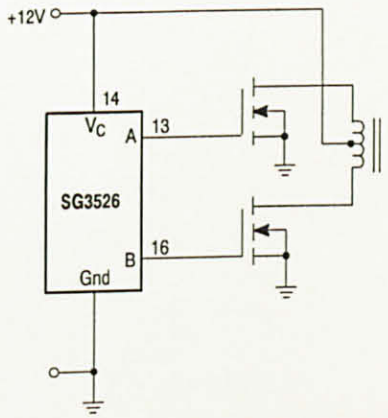



**Figure 17. Soft–Start Circuity**




The totem pole output drivers of the SG3526 are ideally suited for driving the input capacitance of power FETs at high speeds.

**Figure 18. Driving VMOS Power FETs**

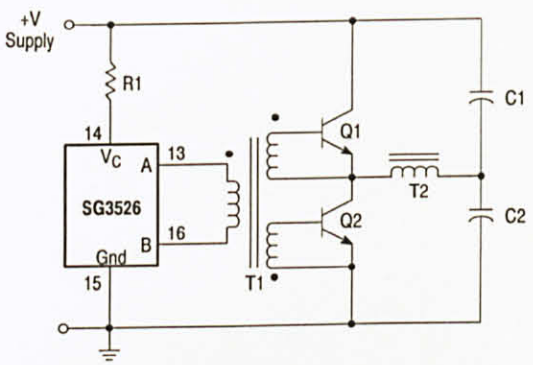
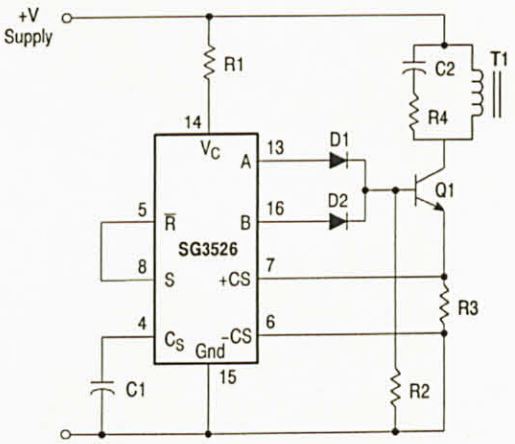



Figure 19. Half–Bridge Configuration




In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

Figure 20. Flyback Converter with Current Limiting

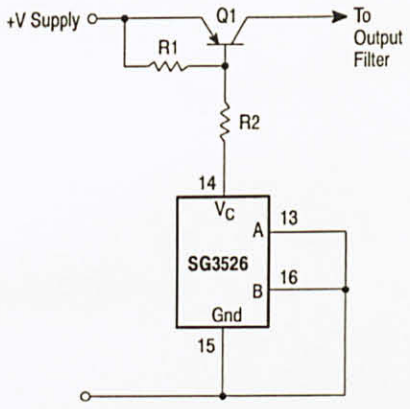



Figure 21. Single–Ended Configuration

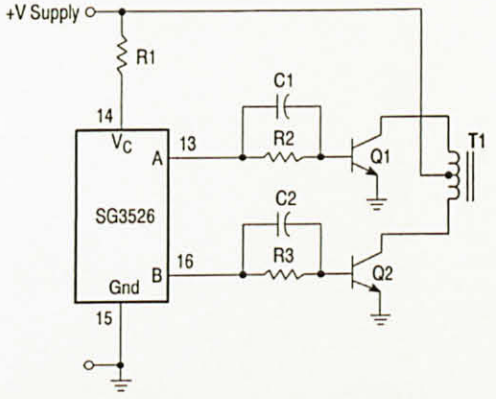
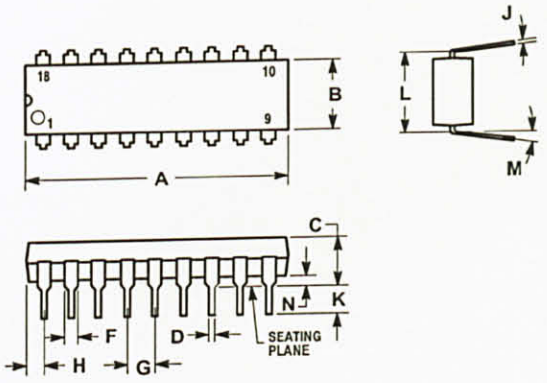



Figure 22. Push–Pull Configuration

## PACKAGE DIMENSIONS

**PDIP–18**
**N SUFFIX**
CASE 707–02
ISSUE D




NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.875 | 0.915 | 22.22 | 23.24 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.140 | 0.180 | 3.56 | 4.57 |
| D | 0.014 | 0.022 | 0.36 | 0.56 |
| F | 0.050 | 0.070 | 1.27 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.040 | 0.060 | 1.02 | 1.52 |
| J | 0.008 | 0.012 | 0.20 | 0.30 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0 ° | 15 ° | 0 ° | 15 ° |
| N | 0.020 | 0.040 | 0.51 | 1.02 |

## Notes

## Notes

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